SONY®

Semiconductor IC

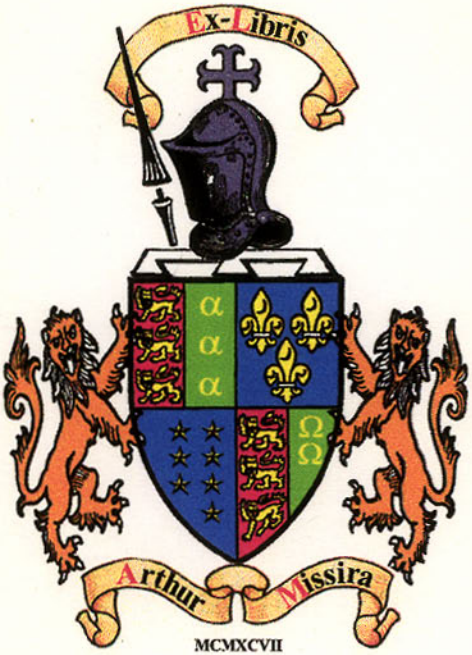
Data Book 1992

Digital Audio ICs

SONY®

Digital Audio ICs

1992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Semiconductor Integrated Circuit Data Book 1992

Semiconductor Integrated Circuit Data Book

1992

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PREFACE

This is the 1992 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

Sony Semiconductor Data Books

The following data books are available for the respective products applications.

1. TV Devices
2. Video Recorder ICs
3. CCD Image Sensors & Peripheral ICs
4. Compact Discplayer ICs
5. Digital Audio ICs
6. Analog Audio ICs
7. Floppy Disk/Hard Disk Drive ICs
8. Radio Communication System ICs
9. A/D, D/A Converters
10. ECL Logic/ASSP ICs
11. Microcomputers
12. Memories
13. Discrete Semiconductors
14. Laser Diodes

In addition, a List of Semiconductor Products covering all manufacutured device on the market, is issued twice a year.

Data books offer information pertaining to the listed products.

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1. List of Model Names

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2. Index by Usage

1) Digital Filter IC

Type	Functions	Page
CXD1244S	For middle class and sophisticated versions, 4/8fs. Filter length 213, 16/18-bit output. Attenuate deemphasis	25
CXD2554M CXD2554P	For popular version, 4/8fs, Filter length 57, 16/18-bit output. Attenuate deemphasis	38
CXD2560M	8fs, Filter length 213, 18/20-bit output. Attenuate, deemphasis	49
CXD2557M	Audio data zero detection	67

2) A/D, D/A Converter

Type	Functions	Page
CXD2552Q	1-bit D/A converter	77
CXD2561BM	1-bit D/A converter, 3rd order noise shaper	85
CXD2555Q	1-bit A/D•D/A converter, Built-in digital filter, 2nd order noise shaper	94

3) ADSP (Audio Digital Signal Processor)

Type	Functions	Page
CXD1160AP CXD1160AQ	Software realized various digital audio data. Double accuracy arithmetic possible	107
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4) Digital Audio Interface IC

Type	Functions	Page
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3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

(1) Conventional nomenclature system

[Example] C X 2 0 0 1 1 A

- Improvement mark
  - "A" is affixed when specifications are partially improved.
- Product number
  - Identifies individual product.
- Category number
  - Indicates the product category in one or two digits.
    - Bipolar IC: 0, 1, 8, 10, 20, 22
    - MOS IC: 5, 7, 23, 79
- Sony IC mark

(2) New nomenclature

[Example] C X A 1 0 0 1 A P

- Package mark
  - P: Plastic Dual In-line Package
  - D: Ceramic Dual In-line Package
  - M: Small Outline L-Leaded Package
  - L: Single In-line Package
  - Q: Quad Flat L-Leaded Package
  - S: Shrink Dual In-line Package
  - N: Very Small Outline Package (SSOP)
  - R: Very Small Quad Flat Package
- Improvement mark
  - "A" is affixed when specifications are improved.
- Product number
  - Identifies the individual product.
- Product category mark
  - A: Bipolar IC
  - B: Bipolar digital IC
  - D: MOS logic IC
  - K: Memory, Mask ROM
  - P, Q: Microcomputer, Microprocessor
  - L: CCD signal processor
- Sony IC mark

(3) Memory nomenclature

[Example] CXK5464AP-□□□□

- Standby current
- Access time
- Package mark
  - P : Dual in-line package
  - D : Ceramic Dual In-line Package
  - SP : Skinny type dual in-line package
  - M : Small outline package
  - J : Small outline J-leaded package
    Quad Flat J-Leaded package
  - TM : Thin small outline package (Normal)
  - YM : Thin small outline package (Reverse)
    (Mirror image pin out)
- Improvement mark
  Improvement mark is affixed when specifications are partially improved.
- Product number
  Identifies the individual product.
- Product category mark
  K: Memory
- Sony IC mark

(4) Microcomputer nomenclature

[Example] CXP5068-□□□□

- Package mark (P, Q, S)
- OEM code
- Product number
  Indentifies the individual product.
- Product category mark
  P: Microcomputer
- Sony IC mark

(5) Hybrid IC nomenclature

[Example] SBX □□□□-□□

- Classification
- Product's number Identifies individual product.
- Sony hybrid IC mark

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

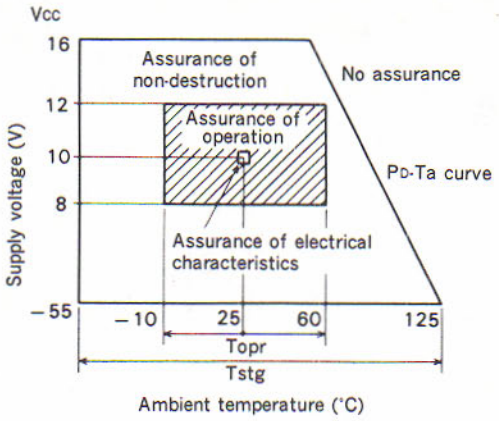
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

A general example on the relation with Absolute Maxium Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

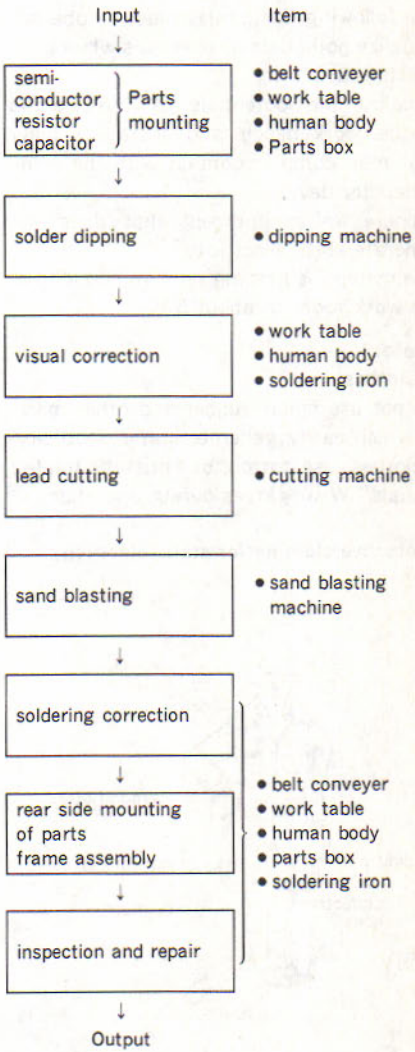
Electrostatic destruction is again drawing people's attention as we are entering the era of LSI, VLSI, and ULSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.

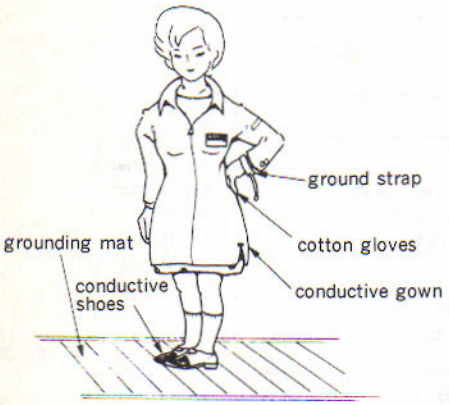
One method is keeping relative humidity in the work room to about 50%.

Operator

(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

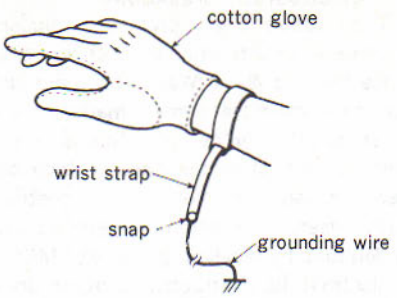
protective clothing for static electricity



(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm.

example of grounding band

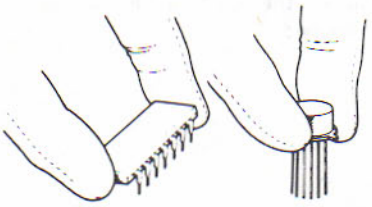


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



Equipment and tools

(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

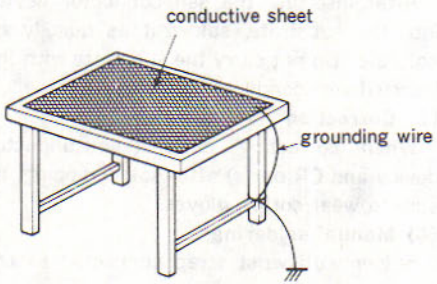
- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

grounding of carrier

(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

grounding of work table



(3) Semiconductor device case

Use a conductive case.

(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

(5) Other points of caution

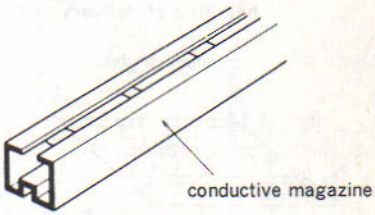
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

Use conductive, or antistatic-treated plastic IC magazines.

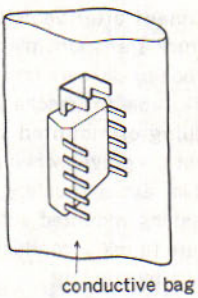
magazine



(2) Bag

Use a conductive bag to store ICs.

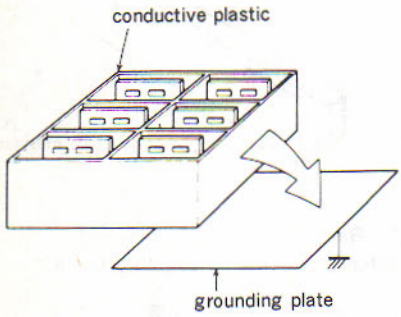
bag



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



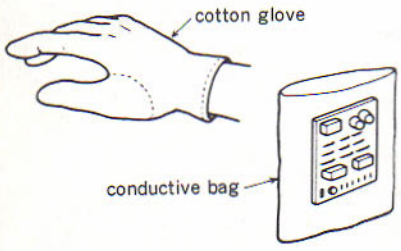
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate

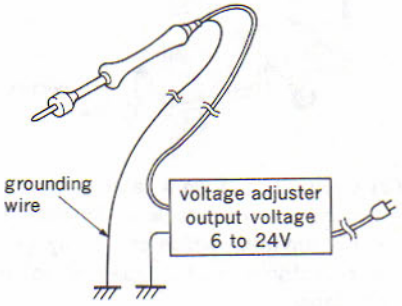


Soldering operation

(1) Soldering iron

Use a soldering iron with a grounding wire and an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

example of solder iron tip grounding



(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves.

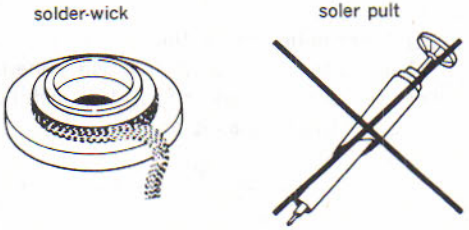
(4) Manual soldering

Solder with wrist strap connected to the hand.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

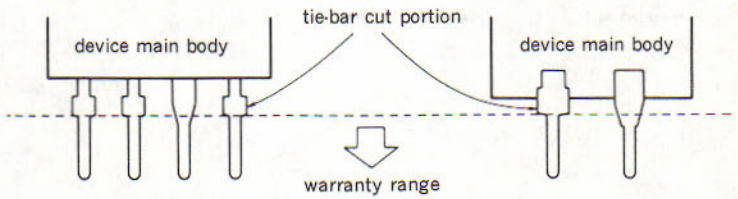
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

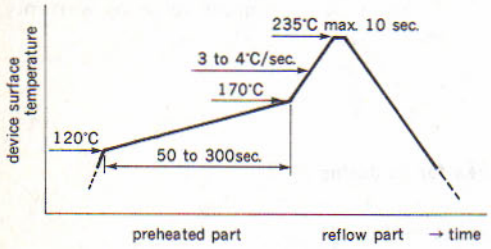
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount devices (SOP, QFP etc) are dipped directly into a solder pot,

the device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

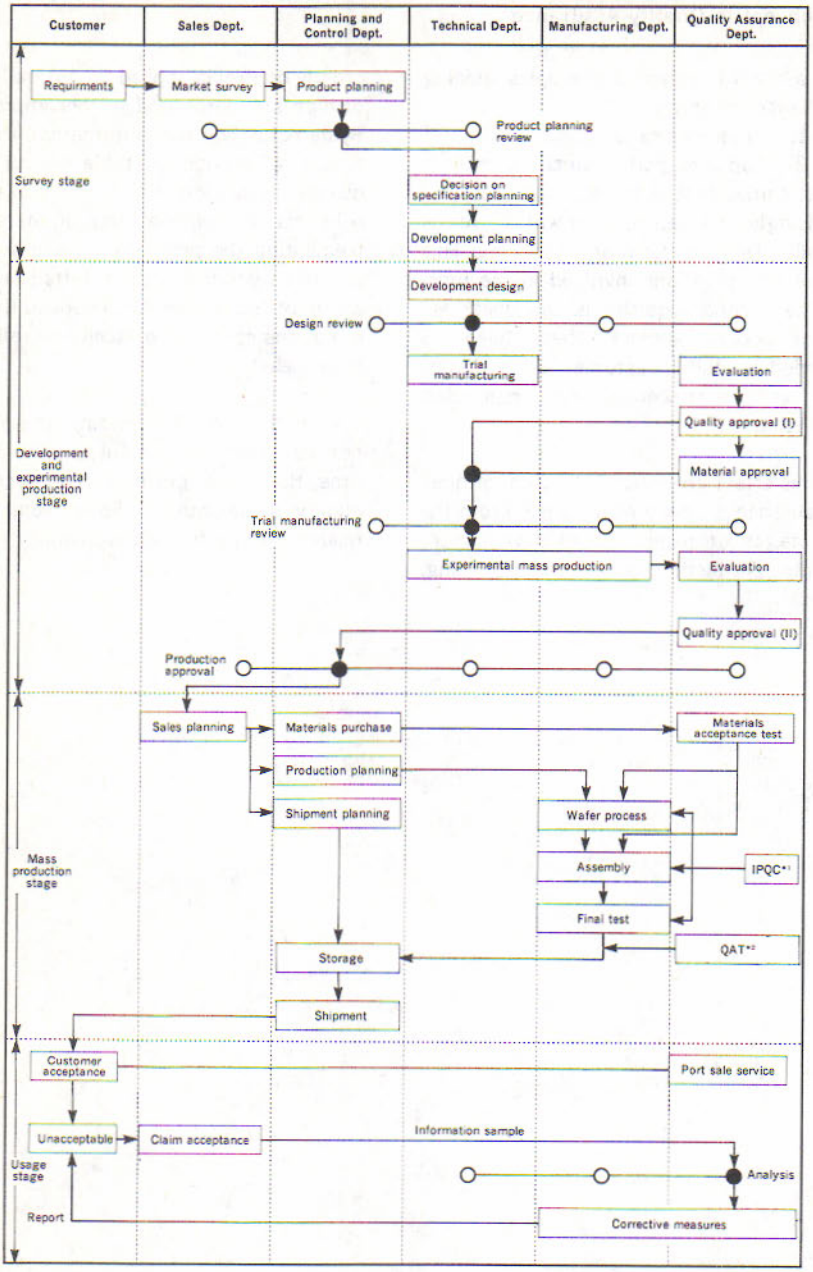
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

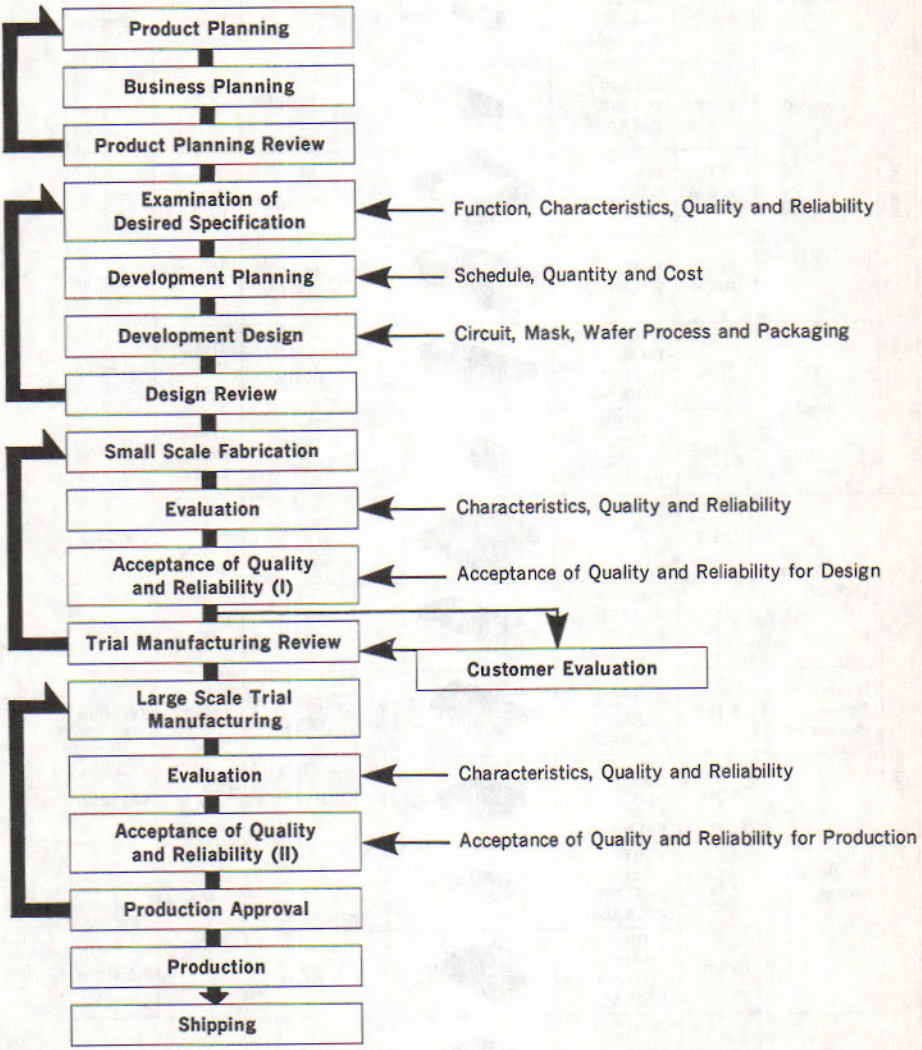
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 203kPa		96h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 15,000m/s² Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 200m/s² 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 200,000m/s² Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

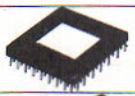
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	Q F J	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic. C·····Ceramic

Digital Filter IC

1) Digital Filter IC

Type	Functions	Page
CXD1244S	For middle class and sophisticated versions, 4/8fs. Filter length 213, 16/18-bit output. Attenuate deemphasis	25
CXD2554M CXD2554P	For popular version, 4/8fs, Filter length 57, 16/18-bit output. Attenuate deemphasis	38
CXD2560M	8fs, Filter length 213, 18/20-bit output. Attenuate, deemphasis	49
CXD2557M	Audio data zero detection	67

SONY

CXD1244S

Digital Filter for CD Player

Description

CXD1244S is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Built-in 4-times/8-times sampling digital filter for 2 channels.
- Ripple within 0.00001dB
- Attenuation within -100dB(24.1k).
- Noise shaping, Attenuator
- Soft muting, de-emphasis and a wide variety of built-in functions.

Application

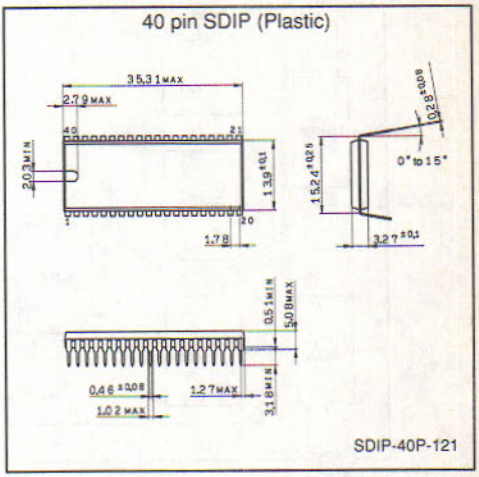
Compact disc player

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	−0.5	to	+6.5	V	
• Input voltage	V_I	−0.5	to	V_{DD} +0.5	V	
• Storage temperature	Tstg	−55	to	+150	°C	
• Allowable power dissipation	P_D			500	mW	(Ta=60°C)

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	−10	to	+60	°C
• OSC frequency	fx	12.0	to	18.5	MHz

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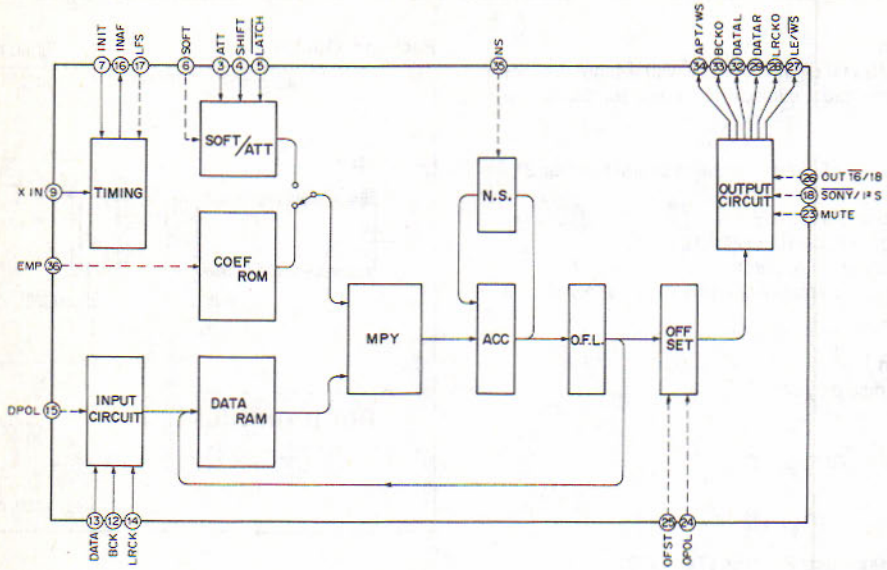
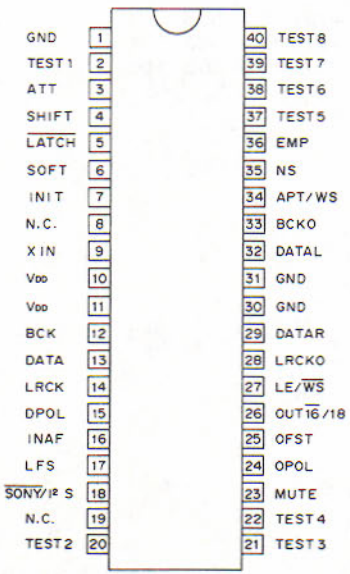
Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	
2	TEST1	I	Test pin (Normally fixed to "L" level)
3	ATT	I	Attenuate data input
4	SHIFT	I	Attenuate data shift clock input
5	LATCH	I	Attenuate data latch clock input
6	SOFT	I	Soft muting ON/OFF active at "H".
7	INIT	I	Synchronous again with the rising edge of this signal.
8	NC		
9	XIN	I	Master CLK input (f=384 Fs)
10, 11	V_{DD}	—	Supply (+5V)
12	BCK	I	BCK input
13	DATA	I	Serial data input (2's complement)
14	LRCK	I	LRCK input
15	DPOL	I	Output data polarity "L" : non inversion "H" : inversion.
16	INAF	O	When I/O sync is missed "H" is output.
17	LFS	I	4Fs mode ON/OFF available at "H" only during I^2S.
18	SONY/I^2S	I	Output format specified at "L": Sony, at "H": I^2S
19	NC	I	
20 to 22	TEST 2 to 4	I	Test pin (Normally fixed to 'L' level)
23	MUTE	I	Turns output to 0 or offset value. Active at 'H'.
24	DPOL	I	Offset polarity 'L': (–) 'H': (+)
25	OFST	I	Offset ON/OFF Active at 'H'
26	OUT16/18	I	Output data word length specified at 'L': 16 bit at 'H': 18 bit
27	LE/WS	O	LE output (Sony format)/WS output (I^2S format)
28	LRCKO	O	LRCKO output
29	DATAR	O	Rch serial data output (2's complement)
30, 31	GND	—	
32	DATAL	O	Lch serial data output (2's complement)
33	BCKO	O	BCKO output
34	APT/WS	O	APT output (Sony format)/WS output (I^2S format)
35	NS	I	Noise shaping ON/OFF Active at 'H'
36	EMP	I	Deemphasis ON/OFF Active at 'H'
37 to 40	TEST 5 to 8	I	Test pin (Normally fixed to 'L' level)

Electrical Characteristics
DC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
'H' input voltage (Except Shift, Latch)	V_{IH}	—	0.76 V_{DD}			V
'H' input voltage (Shift, Latch)						
'L' input voltage (Except Shift, Latch)	V_{IL}	—			0.24 V_{DD}	V
'L' input voltage (Shift, Latch)						
Input leak voltage	I_{LI}	—			±5	µA
'H' output voltage	V_{OH}	I_O=−2mA	V_{DD}−0.5			V
'L' output voltage	V_{OL}	I_O= 2mA			0.4	V

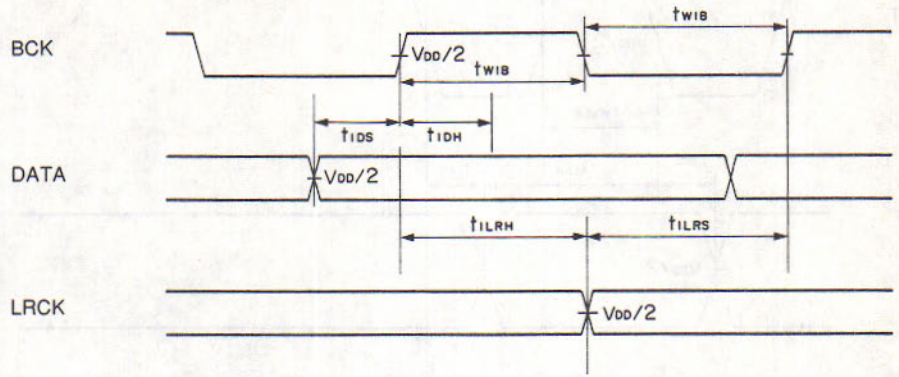
AC characteristics

Item	Symbol	Conditions	Min.	Typ.	Min.	Unit
OSC frequency	Fx		12.0	16.9	18.5	MHz
Input BCK frequency	F_{BCX}				2.31	MHz
Input BCK pulse width	t_{WIB}	Defined at Duty	40*	50	60	%
Input data set up time	t_{IDS}		20			ns
Input data hold time	t_{IDH}		20			ns
Input LRCK set up time	t_{ILRS}		50			ns
Input LRCK hold time	t_{ILRH}		50			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		25			ns
Output data hold time	t_{ODH}		25			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I²S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		35			ns
Output data hold time	t_{ODH}		35			ns
Output BCK pulse width	t_{WOB}	Fx=18.5MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		20			ns
Output data hold time	t_{ODH}		20			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I²S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		32			ns
Output data hold time	t_{ODH}		32			ns
Output signal Rise/Fall time	t_R, t_F	CL=50pF			30	ns

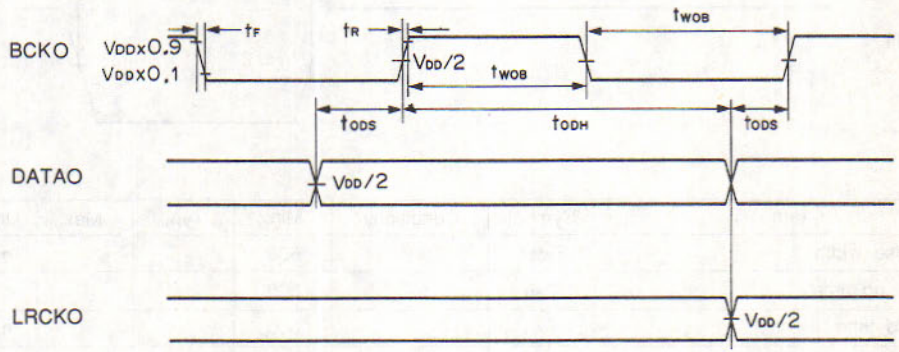
Note) Duty defined at 1/2 VDD, see the Timing Chart.

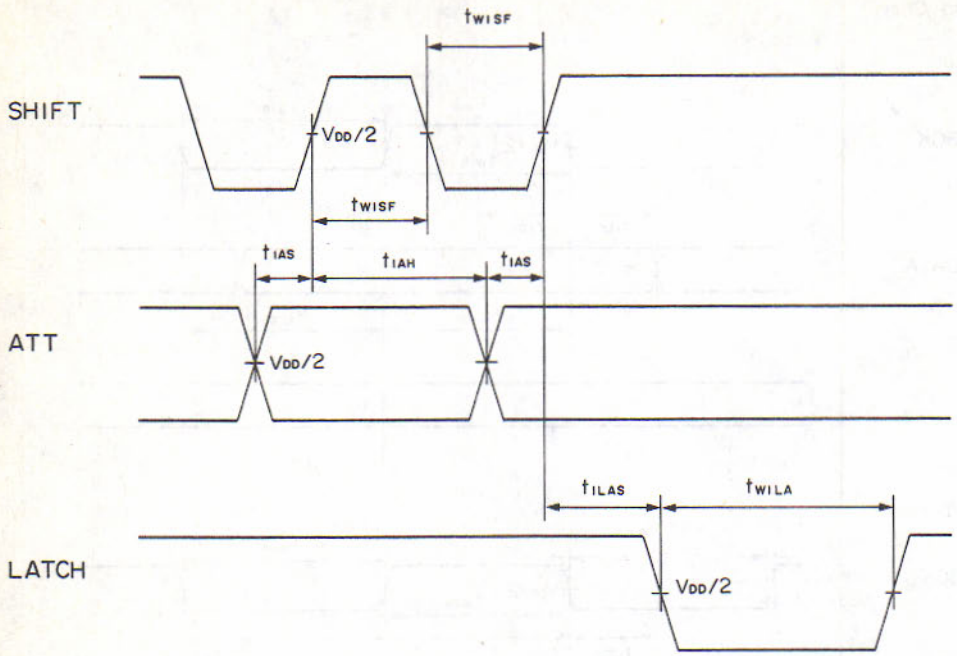
Timing Chart

- Input



- Output





Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift pulse width	T_{WISF}		600			ns
ATT set up time	T_{IAS}		300			ns
ATT hold time	T_{IAH}		600			ns
Latch pulse width	T_{WILA}		400			ns
Latch set up time	T_{ILAS}		500			ns

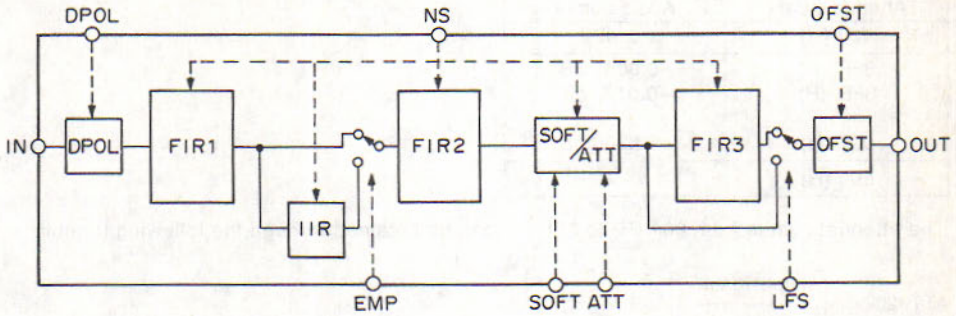
Schmitt input characteristics (SHIFT, LATCH)

	Min.	Typ.	Max.	Unit
V_{T+}	0.54×V_{DD}	3.0	0.76×V_{DD}	V
V_{T-}	0.24×V_{DD}	2.0	0.43×V_{DD}	V
HYST	0.52	1.0	———	V

Functions

Conceptual block diagram

An outline block diagram of this LSI is shown below.

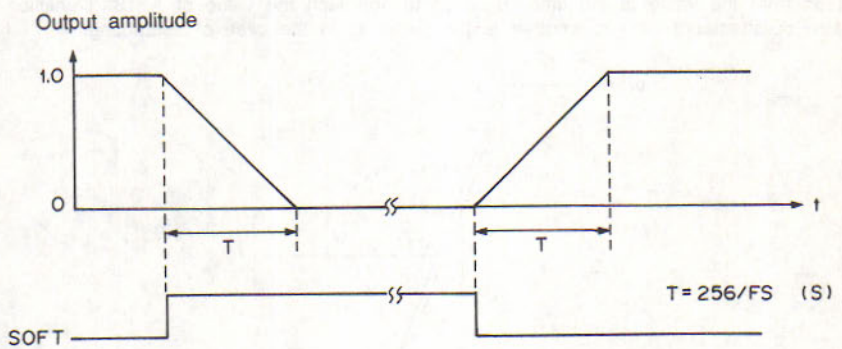


1. Noise shaping

For respective outputs FIR 1 to 3, IIR, SOFT/ATT figures are usually rounded off. However, by turning NS to "H" noise shaping can be applied.
NS register is cleared when INIT is at "L" or NS at "L".

2. Soft muting

By turning SOFT to "H"/"L", data can be smoothly muted or demuted.



3. Digital attenuator

Can attenuate output data by means of transfer data from an external microcomputer.

1) Command and Audio output
Attenuate data is in 12 bit and can be set in 1024 steps.
The relationship between command and output is shown in the chart below.

Attenuate data	Audio output
400 (H)	0 dB
3FF (H)	-0.0085 dB
3FE (H)	-0.017 dB
⋮	⋮
001 (H)	-60.206 dB
000 (H)	-∞

The attenuate value from 001 (H) to 3FF (H) can be obtained through the following formula.

$$ATT = 20\log\left[\frac{\text{Input data}}{1024}\right] \text{dB}$$

Example: Attenuate data for 3FA (H)

$$ATT = 20\log\left[\frac{1018}{1024}\right] \text{dB} = -0.051 \text{ dB}$$

2) Attenuator operation
Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that ATT1>ATT3> ATT2 and that the place of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before. The value of ATT2 is reached (during the state of A in Fig.1),the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of softmuting.

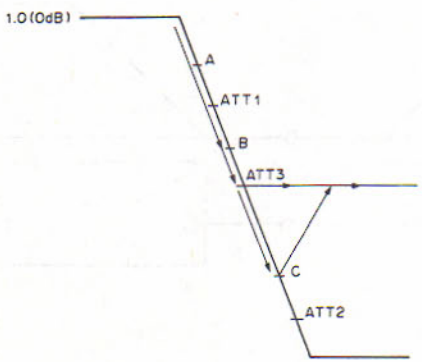
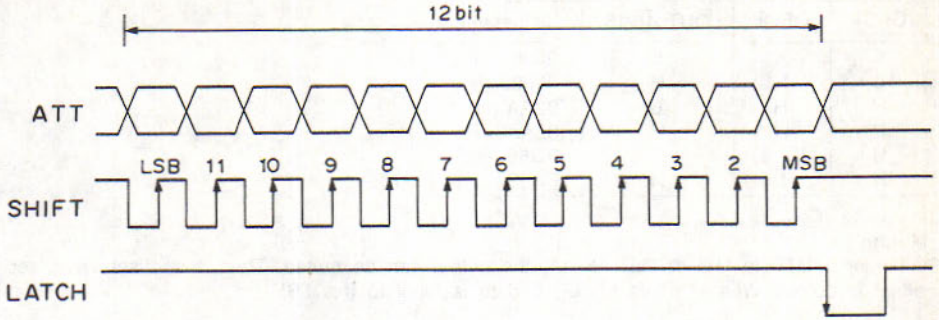
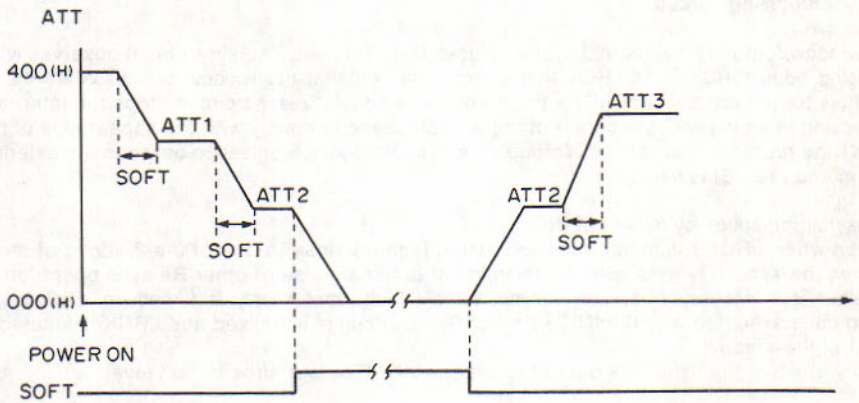


Fig.1 Transition from one attenuator value to another

3) Input data timing
Attenuate function can be activated by means of ATT, Shift and Latch.
Transfer format is indicated as follows.



(1) ATT data is a 12 bit word length and LSB first transfer ATT data is available 000(H) to 400(H).
(2) When Latch is at "L", ATT cannot be transferred.
(3) With INIT at ƒ, 400 (H) is set as ATT data.



- The transition from ATT1 to ATT2 takes place in soft muting operation.
- During attenuate operation SOFT is set to either ON or OFF, it turns back to the original ATT data.
- When ATT data =400 (H) Noise shaping is not applied regardless of NS ON or OFF.
  When ATT data =400 (H) Noise shaping is applied regardless of NS ON or OFF.

4. Digital deemphasis
By turning EMP to "H", deemphasis can be applied by means of IIR filter.
Time constant of de-emphasis are τ_1=50μs and τ_2=15μs at f_s=44.1kHz.

5. Offset

Offset can be applied to the output data by means of OFST and OPOL.
Pos/Neg selection of the offset value is possible as indicated in the following chart.

OFST	OPOL	OUT $\overline{16}$/18	Offset value
L	X	L	0000 (H)
L	X	H	00000 (H)
H	H	L	02AA (H)
H	H	H	02AA8 (H)
H	L	L	FD55 (H)
H	L	H	FD554 (H)

6. Muting

By turning MUTE to "H" or INIT to "L", the output can be muted. Then, the offset value set at the offset is output. When INIT is at "L", 0 data is input to this LSI.

7. Data polarity

Inversion and non inversion of the output data can be selected by means of DPOL.
When DPOL is at "H", non inversion.
when DPOL is at "L", inversion.

8. I/O synchronizing circuit

1) Principle

A window featuring 10 internal system clocks (XIN/2) is set. The sync circuit observes whether the rising edge (LRCK f) of LRCK that is input, has entered the window or not. When the power supply is turned on, should LRCK f be out of the window the sync circuit stops the internal processing in timing with the center of the window. Synchronously with the appearance of the next LRCK f the processing is started. Through this operation synchronization between the exterior system and this LSI is established.

2) Resynchronization by means of INIT

Even when LRCK f is inside the window but located close to one of the 2 edges of the window, the sync may miss with the mingling of external noise or other Re sync operation. To this effect it is necessary to apply resync, without fault, after supply is turned on. ReSync operation is executed with the INIT f timing. Sync. circuit is initialized and LRCK is located in the center of the window.
Moreover, when the sync falls out of the window, INAF output turns to "H" level.

3) Non synchronous MUTE

When INAF is at H, 0 data is output regardless of offset ON/OFF.

9. Output format

The output format of this LSI can be selected as shown in the chart below.

	8Fs		4Fs
	SONY	I²S	I²S
(Control pin)			
$\overline{\text{SONY}}$/I2S	'L'	'H'	←
LEFS	no effect	'L'	'H'
OUT$\overline{16}$/18	At will	no effect	←
(Output pin)	8LRCK	4LRCK	←
LRCKO	24BCK	16BCK	←
BCKO	DATAL	Staggered	MIX data
DATAL	DATAR	DATA	'L'
DATAR	APT	WS	←
APT/WS			
LE/$\overline{\text{WS}}$	LE	$\overline{\text{WS}}$	←

10. I/O signal latch timing

1) Input

DPOL, SOFT, MUTE, OFST, OPOL, INIT, $\overline{\text{SONY}}$/I²S, LFS, OUT$\overline{16}$/18, NS, EMP

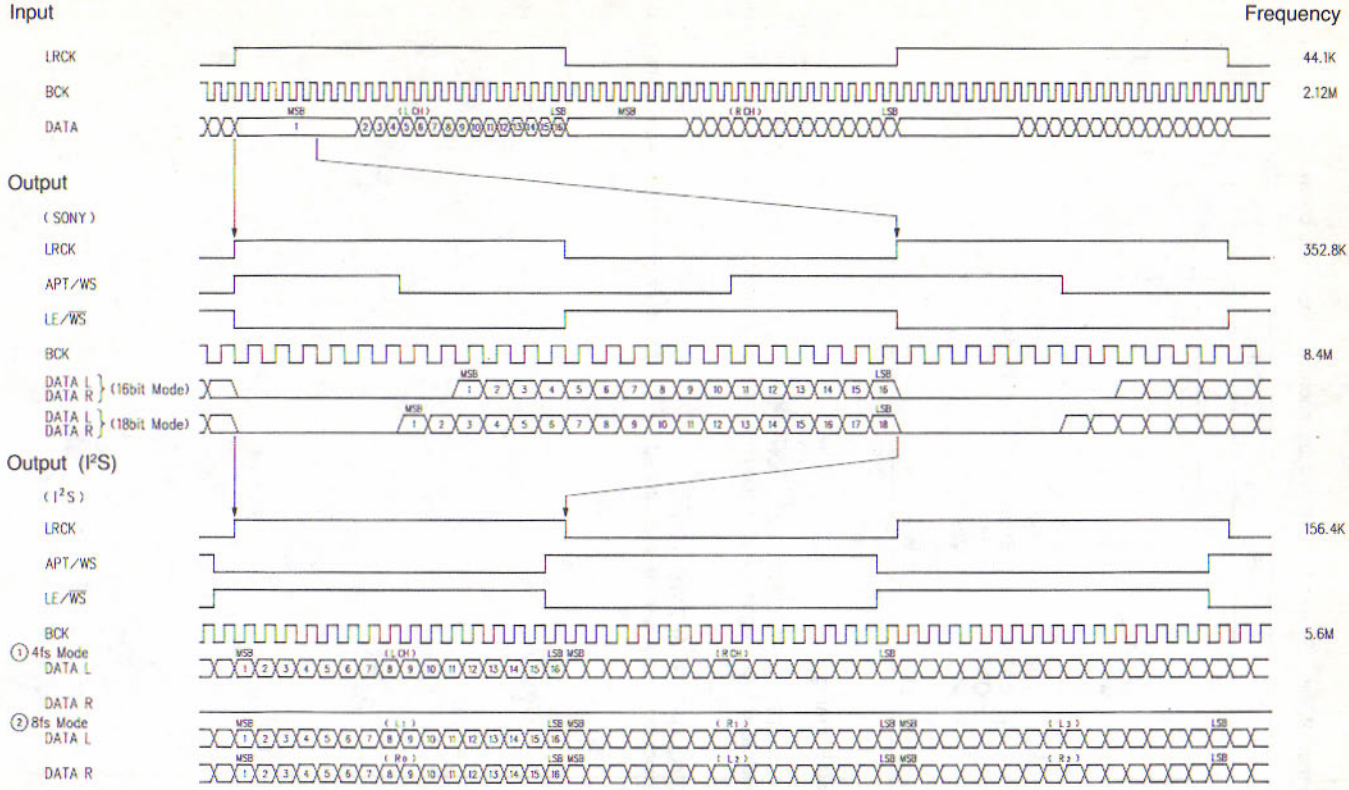
The above indicated input signals are latched by means of internal clocks equivalent to LRCK.

2) Output

LRCKO, DATAL, DATAR, APT.WS, LE/$\overline{\text{WS}}$

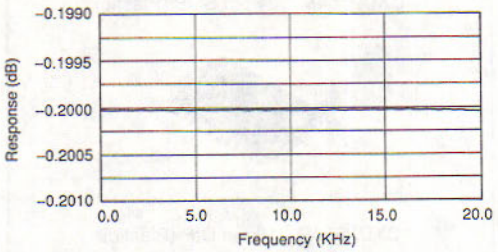
The above indicated output signals are latched by means of internal clocks equivalent to BCKO.

I/O Timing Chart

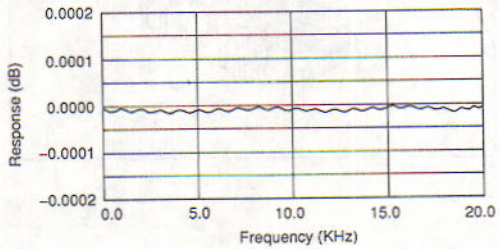


Filter characteristics (for 4Fs)

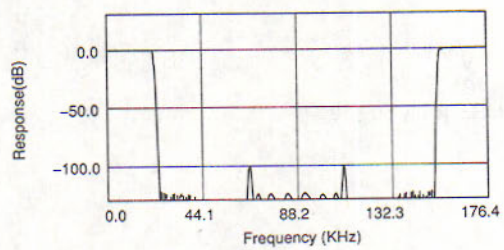
Frequency characteristics



Ripple characteristics

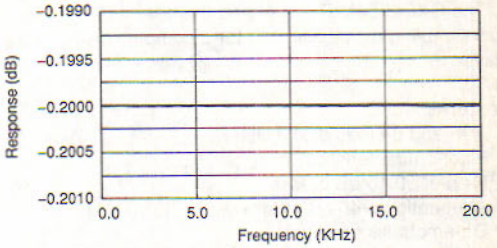


Attenuate

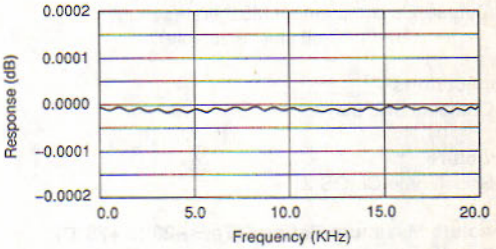


Filter characteristics (for 8Fs)

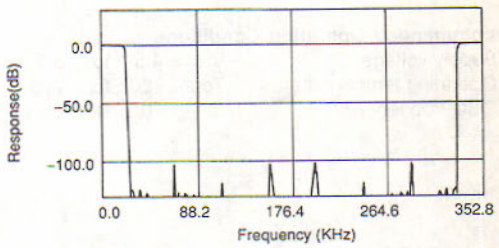
Frequency characteristics



Ripple characteristics



Attenuate

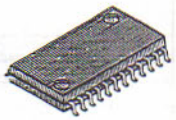


SONY®

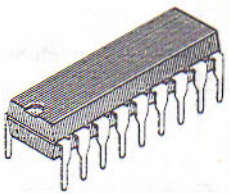
CXD2554M/P

Digital Filter for CD

CXD2554M 24 pin SOP (Plastic)



CXD2554P 18 pin DIP (Plastic)



Description

The CXD2554M/P is a 4- and 8-times oversampling digital filter LSI for a compact disc player.

Features

- A 4- and 8-times digital filter
- Filter characteristics
  Ripple: ±0.15 dB or less
  Attenuation: −40 dB or less
- De-emphasis function
- Attenuating function (Built-in 1st noise shaper)
- Digital offset function
- I/O format
  Input: 2's complement MSB first (serial)
  Output: 2's complement MSB first (serial)
  (16- or 18-bit slot selectable)

Applications

Compact disc player

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = −20 to +75°C)

• Supply voltage	V_{DD}	−0.5	to	+6.5	V	
• Input voltage	V_I	−0.5	to	V_{DD} +0.5	V	
• Allowable power dissipation	P_D		500		mW	(Ta = 75°C)
• Storage temperature	Tstg	−55	to	+150	°C	

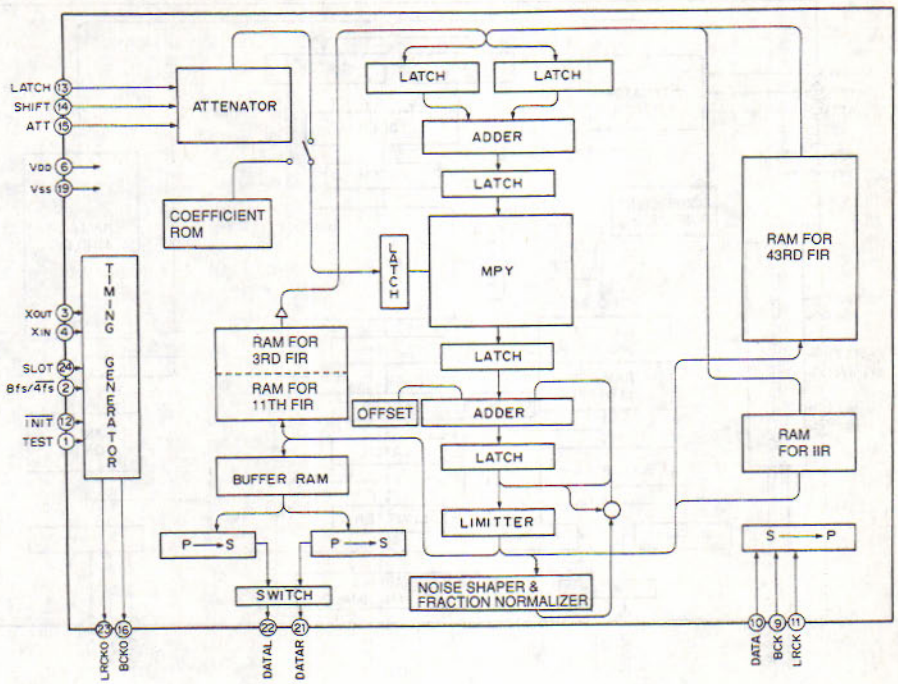
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5	to	5.5	V	
• Operating temperature	Topr	−20	to	+75	°C	
• OSC frequency	fx	10	to	20	MHz	(Duty 50 ±10%)

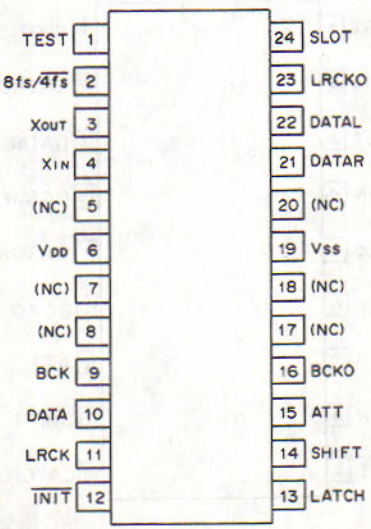
E90330B0Z-YA

CXD2554M

Block Diagram

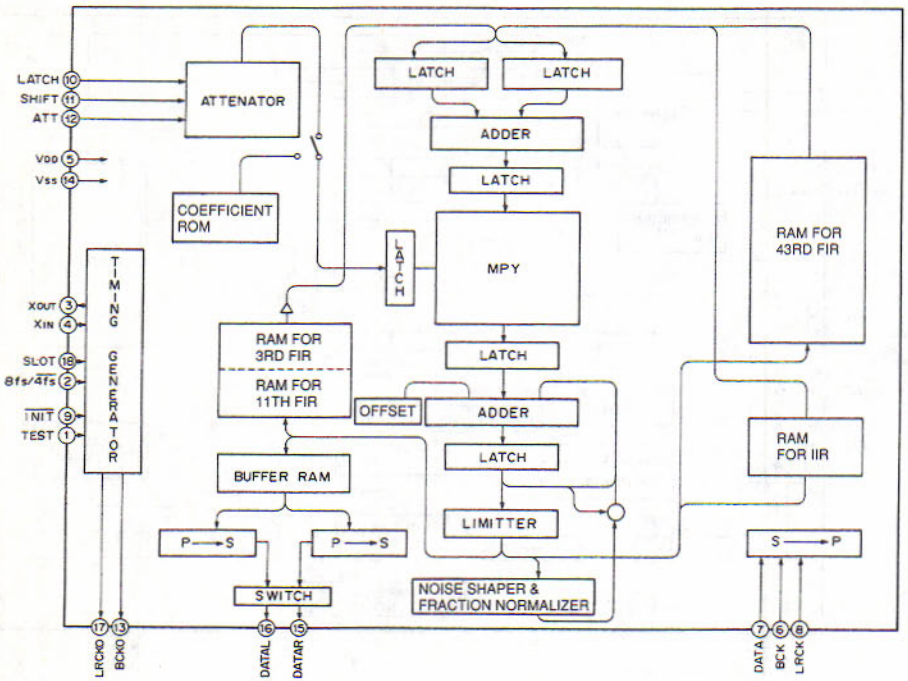


Pin Configuration

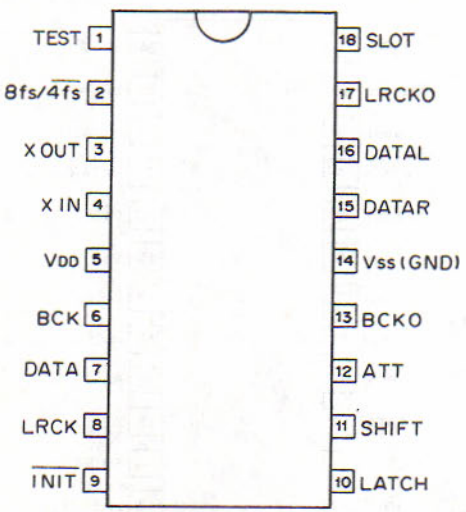


CXD2554P

Block Diagram



Pin Configuration



Pin Description

Pin No.		Symbol	I/O	Description
CXD2554P	CXD2554M			
1	1	TEST	I	Test pin. Fixed at 'L' level in normal operation mode.
2	2	8fs /4fs	I	To specify FIR 3. 'H': 8fs 'L': 4fs
3	3	XOUT	O	Master clock output (f = 384fs)
4	4	XIN	I	Master clock input (f = 384fs)
5	6	V_{DD}	–	Power supply (+5 V)
6	9	BCK	I	BCK input
7	10	DATA	I	Serial data input (2's complement)
8	11	LRCK	I	LRCK input
9	12	$\overline{INIT}$	I	Re-synchronized by rising edge of this signal
10	13	LATCH	I	Latch clock input
11	14	SHIFT	I	Shift clock input
12	15	ATT	I	Attenuate data input
13	16	BCKO	O	BCK output
14	19	V_{SS} (GND)	–	Power supply (0 v)
15	21	DATAR	O	4fs mode: WCK output 8fs mode: RCH serial data output (2's complement)
16	22	DATAL	O	4fs mode: LCH and RCH time division serial data output (2's complement) 8fs mode: LCH serial data output (2's complement)
17	23	LRCKO	O	LRCK output
18	24	SLOT	I	To specify output slot. 'H': 18-bit slot 'L': 16-bit slot
–	5, 7, 8, 17, 18, 20	(NC)	–	No connection

* TEST, 8fs /4fs and SLOT pins: Pull down resistance

Electrical Characteristics

DC characteristics (V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C)

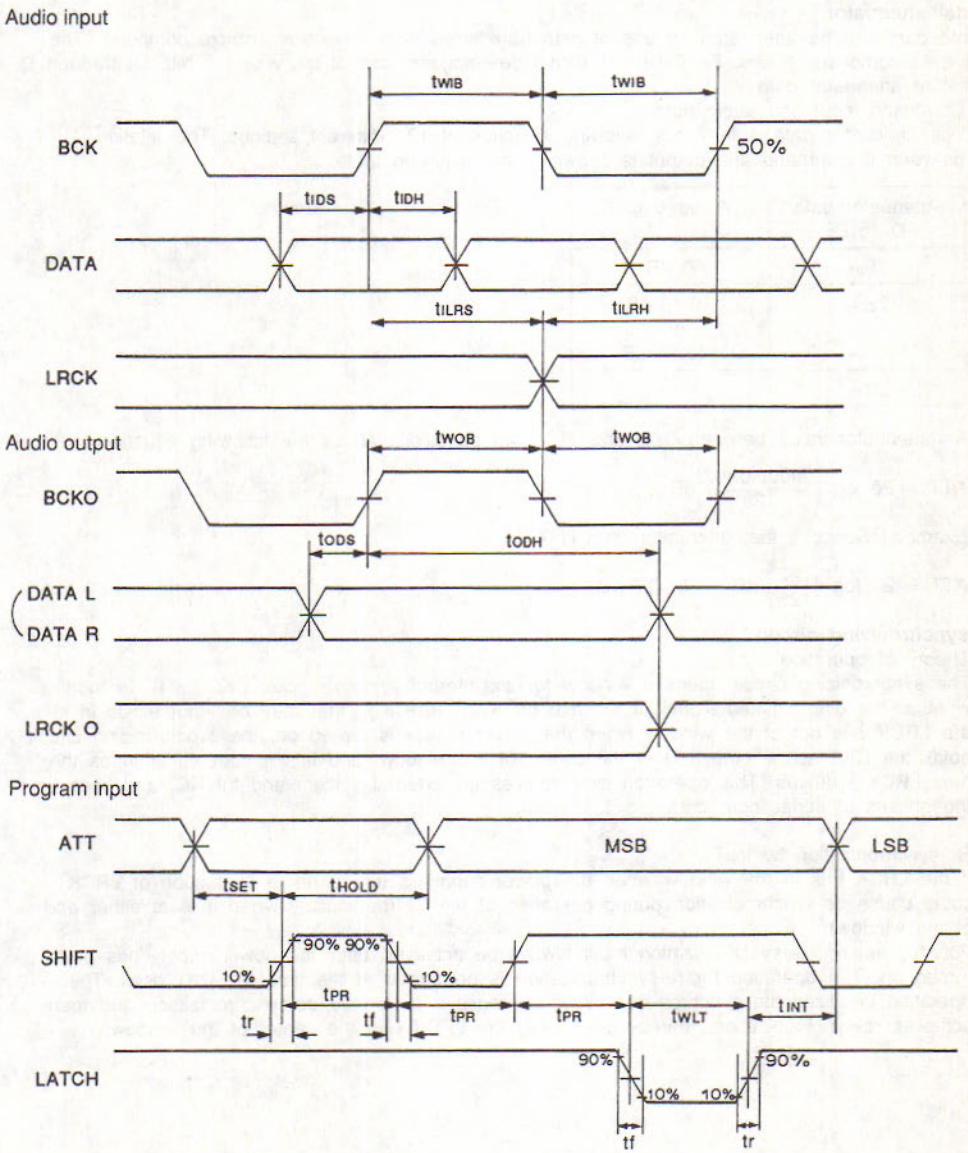
Pin	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
All inputs except XIN	Input capacitance	C_{IN}	——	–	3	5	pF
Note 1	"H" input voltage	V_{IH}	——	0.76 V_{DD}	–	–	V
	"L" input voltage	V_{IL}	——	–	–	0.24 V_{DD}	
Note 2	Input leak current 1	I_{ILK1}	V_I = V_{DD}/0V	–	–	±5	µA
TEST, 8fs /4fs, SLOT	Pull down resistance	R_{PD}	——	7.5	15	30	kΩ
	"L" input leak current	I_{IL}	V_I = 0V	–	–	5	µA
XIN	Input leak current 2	I_{ILK2}	V_I = V_{DD}/0V	–	–	±20	
BCKO, DATAR, DATAL, LRCKO	"H" output voltage	V_{OH}	I_D = −4 mA	V_{DD}-0.5	–	–	V
	"L" output voltage	V_{OL}	I_D = 4 mA	–	–	0.4	
	Consumption current	I_{DD}	When no load is placed V_I = V_{DD}/0V fx = 16.9344 MHz	–	–	40	mA

Note 1) TEST, 8fs /4fs, BCK, DATA, LRCK, INIT, LATCH, SHIFT, ATT, SLOT
Note 2) BCK, DATA, LRCK, INIT, LATCH, SHIFT, ATT

AC characteristics (V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fx	——	10	16.9344	20	MHz
Input BCK frequency	f_{BCK}		–	–	4.0	
Input BCK pulse width	t_{WIB}	——	100	–	–	ns
Input data set-up time	t_{IDS}	——	20	–	–	
Input data hold time	t_{IDH}	——	20	–	–	
Input LRCK set-up time	t_{ILRS}	——	50	–	–	
Input LRCK hold time	t_{ILRH}	——	50	–	–	
Output BCKO pulse width	t_{WOB}	8fs	40	–	–	
Output data set-up time	t_{ODS}	fx = 16.9344 MHz	25	–	–	
Output data hold time	t_{ODH}	C1 = 50 pF	25	–	–	
Program input base time	t_{PR}	fx = 16.9344 MHz	250	–	–	
Latch input pulse width	t_{WLT}		500	–	–	
Rise time (SHIFT, LATCH)	tr		–	–	200	ns
Fall time (SHIFT, LATCH)	tr		–	–	200	
Set-up time (ATT)	t_{SET}	——	500	–	–	
Hold time (ATT)	t_{HOLD}		500	–	–	
Interval	t_{INT}		1000	–	–	

Timing Chart



Description of Functions

A. Soft muting

The soft mute function mutes or demutes output data on the basis of a muting time of 1024/fs (CD: fs = 44.1 kHz).

B. Digital attenuator

Output data can be attenuated by use of data transferred from an external micro computer. The ATT data comprises 8 bits. Bit D_7 is the digital de-emphasis control bit, whereas bits D_6 through D_0 constitute attenuator data.

(1) Command input and audio output

The attenuator data is in 7 bits, allowing selection of 127 different settings. The relation between a command and output is shown in the following table.

Attenuator data D_6 to D_0	Audio output
$7F_{(H)}$	0 dB
$7E_{(H)}$ to $01_{(H)}$	−0.13 dB to −42.144dB
$00_{(H)}$	$-\infty$

An attenuator value between $01_{(H)}$ and $7E_{(H)}$ can be calculated by the following equation.

$$ATT = 20 \log \left(\frac{\text{Input data}}{128} \right) dB$$

Example) Suppose that attenuator data is 7A.

$$ATT = 20 \log \left(\frac{122}{128} \right) dB = -0.417 \text{ dB}$$

C. I/O synchronizing circuit

1) Theory of operation

The synchronizing circuit opens a window for six internal system clocks, CK2 (fx/4), to monitor whether the differentiated signal of the rise of LRCK (LRCK f) that may be input exists in it. If the LRCK f is out of the window when the power supply is turned on, the synchronizing circuit holds the CK2 at the time it is in the center of the window, and lets it start as soon as the next LRCK f arrives. This operation synchronizes an external system and this IC, and lines up the phases of serial input data.

2) Re-synchronization by $\overline{\text{INIT}}$

If the LRCK f is in the window when the power supply is turned on, a fluctuation of LRCK could cause de-synchronization during operation of the IC (particularly when it is at either end of the window).

For this reason, re-synchronization must always be achieved after the power supply has been turned on. The operation for re-synchronization is performed at the time the $\overline{\text{INIT}}$ rises. The operation initializes the synchronizing circuit to cause a temporary de-synchronization and then achieves re-synchronization, thereby positioning the LRCK f in the center of the window.

D. Attenuator operation

Suppose that there are three pieces of attenuator data, ATT1, ATT2 and ATT3 and that their relations are ATT1>ATT3>ATT2. Assume that ATT1 is transferred first, followed by ATT2.
If ATT2 is transferred before the value of ATT1 is reached (during the state of A in Fig. 1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig. 1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of soft muting.

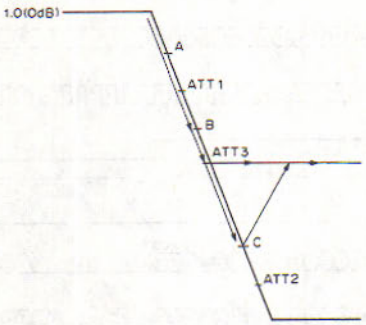


Fig. 1 Transition from one attenuator value to another

E. Input data timing

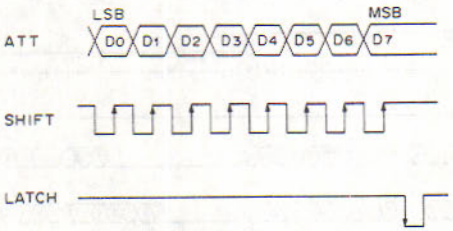


Fig. 2 Timing of ATT, SHIFT and LATCH

① ATT data is configured on the LSB first basis.
② ATT data
D_7 : Digital de-emphasis control bit
H: Emphasis ON
L: Emphasis OFF
Note that emphasis time constants are τ_1 = 50 µs and τ_2 = 15 µs at fs = 44.1 kHz.
D_0 to D_6: Attenuator data

F. About $\overline{\text{INIT}}$ pin is $\int$

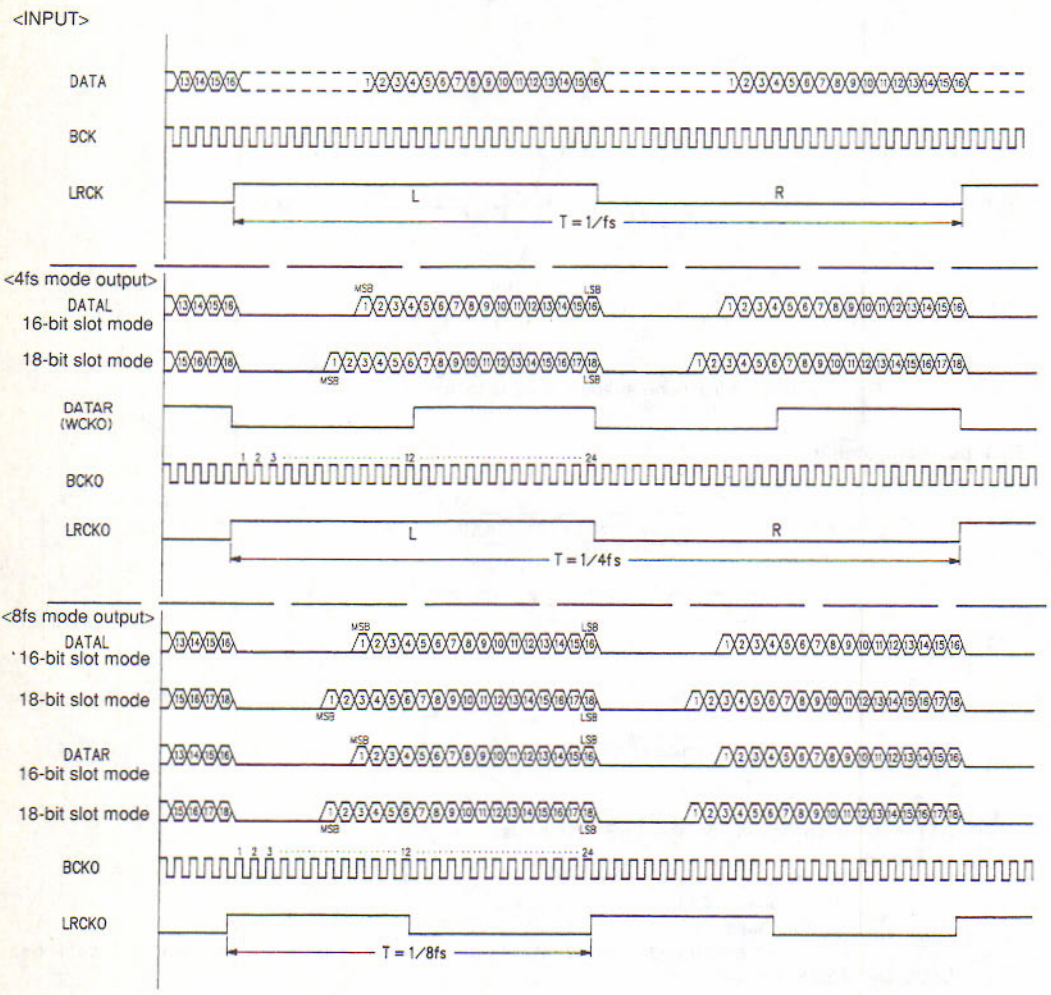
After $\overline{\text{INIT}}$ is $\int$, the counters and registers for the attenuators in the IC are set at $7F_{(H)}$.

G. Digital offset

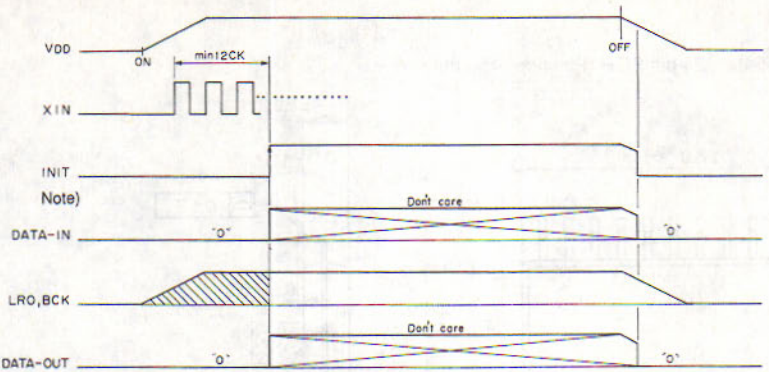
An offset value is added to the digital filter output. The value is $02AA_{(H)}$ in the 16-bit slot mode and $02AA0_{(H)}$ in the 18-bit slot mode.

In the muting mode, this offset value triggers muting.

I/O timing



Operation in POWER ON/OFF state

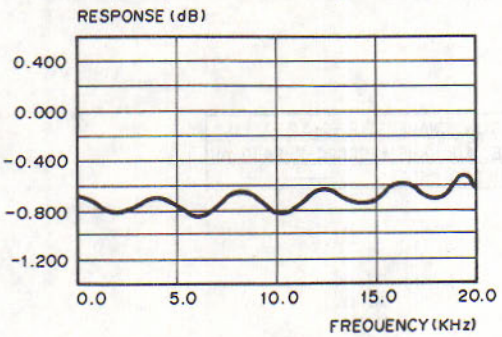


Note) To initialize first turn on power. After V_{DD} reaches 4.5V and the IC stabalizes (V_{DD} levels off), input at least 12 CKs to XIN. Bringing INIT "H" completes initialization.

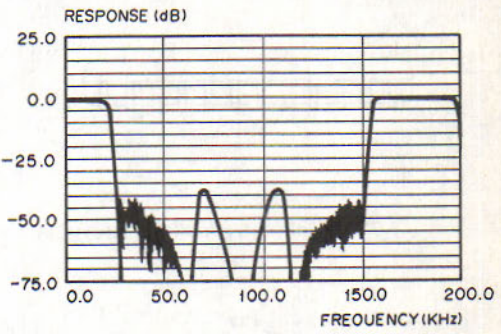
Filter Characteristics

Quadrupled oversampling mode

Frequency Characteristics 1 (Pass band)

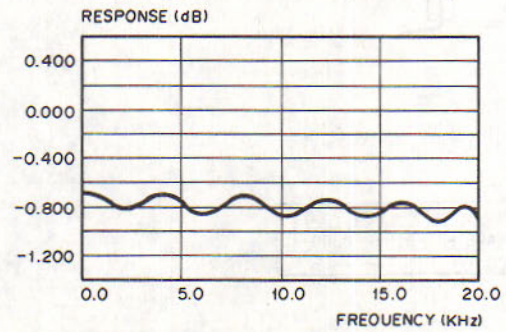


Frequency Characteristics 2 (Stop band)

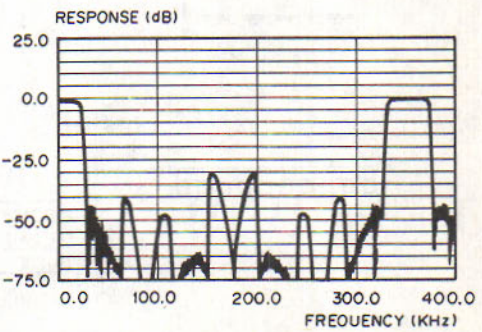


Octupled oversampling mode

Frequency Characteristics 1 (Pass band)

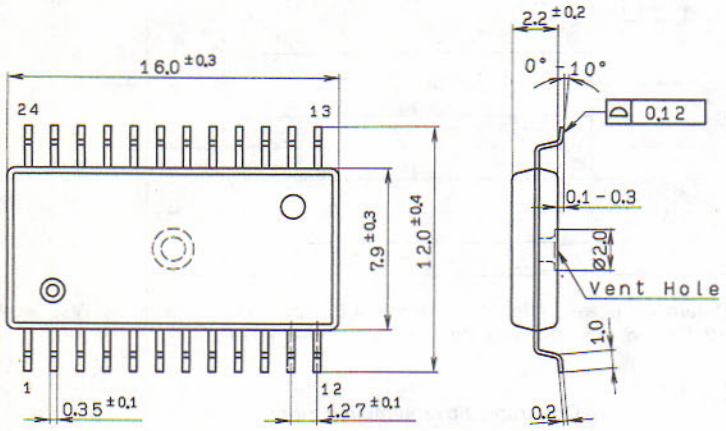


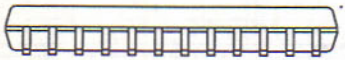
Frequency Characteristics 2 (Stop band)



Package Outline Unit: mm

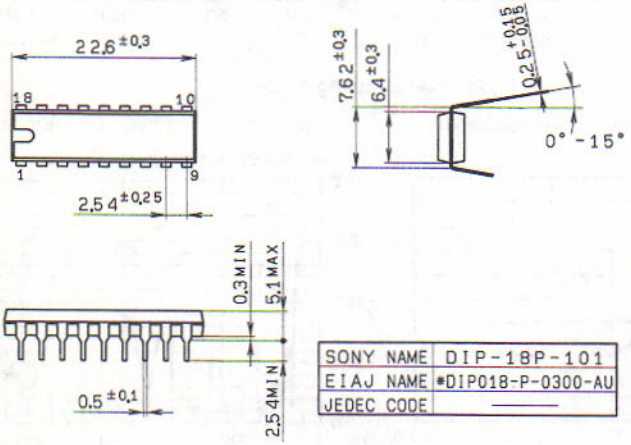
CXD2554M 24 pin SOP (Plastic) 450 mil





SONY NAME	SOP-24P-L101
EIAJ NAME	*SOP024-P-0450-AU
JEDEC CODE	

CXD2554P 18 pin DIP (Plastic) 300 mil



SONY NAME	DIP-18P-101
EIAJ NAME	*DIP018-P-0300-AU
JEDEC CODE	

SONY

CXD2560M

Digital Filter for Audio Applications

Description

The CXD2560M is an 8-times oversampling digital filter LSI for digital audio applications. It features built-in dual filters for both left and right channels as well as a noise shaper, attenuator, soft-muting, and de-emphasis controls.

Features

- Built-in 8-times oversampling digital filters for both channels.
- Filter characteristics
  Ripple: ± 0.00001dB or less (0 to 20k)
  Attenuation: –100dB or less (24.1k to)
- Noise shaper, attenuator, sort-muting and de-emphasis functions
- I/O format
  Input : 2's complement MSB/LSB first (serial)
  (16-bit or 18-bit slot selectable)
  Output: 2's complement MSB/LSB first (serial)
  (18-bit or 20-bit slot selectable)

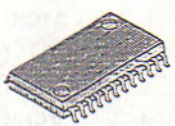
Applications

CD, DAT, BS tuner, and digital amplifiers

Structure

Silicon-gate CMOS IC

24 pin SOP (Plastic)



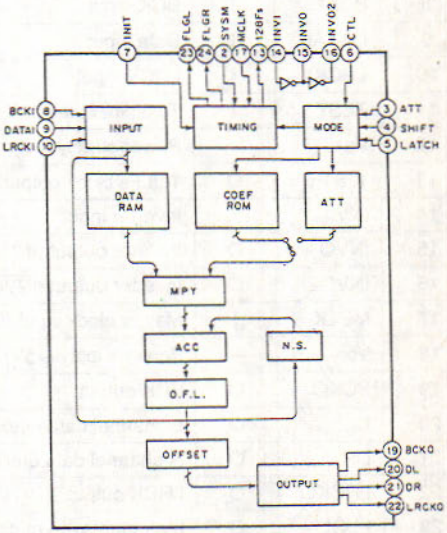
Absolute Maximum Ratings (Ta = 25 °C)

• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	VI	–0.3 to V_{DD}+0.3	V
• Allowable power dissipation	P_D	500 (Ta=+75 °C)	mW
• Storage temperature	Tstg	–50 to +150	°C

Recommended Operating Conditions

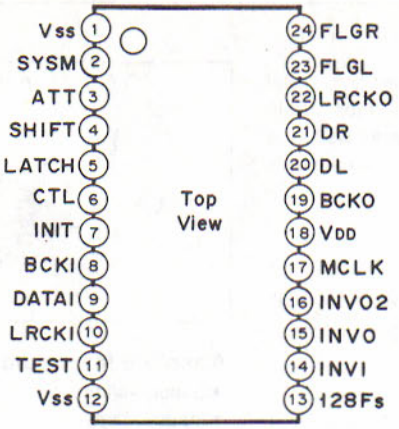
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C
• OSC frequency	fx	15 to 27	MHz

Block Diagram



E91411A22-ST

Pin Configuration (Mini-flat package)



Pin Description

Pin No.	Symbol	I/O	Description
1	Vss	——	Power supply (0V)
2	SYSM	I	System mute input. "H": FLGL and FLGR outputs active.
3	ATT	I	When CTL "L": ATT data input. CTL "H": EMP input.
4	SHIFT	I	When CTL "L": shift clock input. CTL "H": FS32 input.
5	LATCH	I	When CTL "L": latch clock input. CTL "H": FS48 input.
6	CTL	I	Fixed internally at "L" level. "H": direct input mode. "L": serial transfer mode.
7	INIT	I	Re-synchronized by rising edge of this signal
8	BCKI	I	BCK input
9	DATAI	I	Data input
10	LRCKI	I	LRCK input
11	TEST	I	Test pin. Fixed at "L" level in normal operation mode.
12	Vss	——	Power supply (0V)
13	128 Fs	O	128 Fs clock output
14	INVI	I	Inverter input
15	INVO	O	Inverter output ($\overline{\text{INVI}}$)
16	INVO2	O	Inverter output ($\overline{\text{INVO}}$)
17	MCLK	I	Master clock input (f=512Fs)
18	VDD	——	Power supply (+5V)
19	BCKO	O	BCK output
20	DL	O	L-channel data output
21	DR	O	R-channel data output
22	LRCKO	O	LRCK output
23	FLGL	O	L-channel zero muting flag output
24	FLGR	O	R-channel zero muting flag output

Electrical Characteristics

DC Characteristics

(V_{DD}= 4.75 to 5.25V, Ta=–20 to +75 °C, GND=0V)

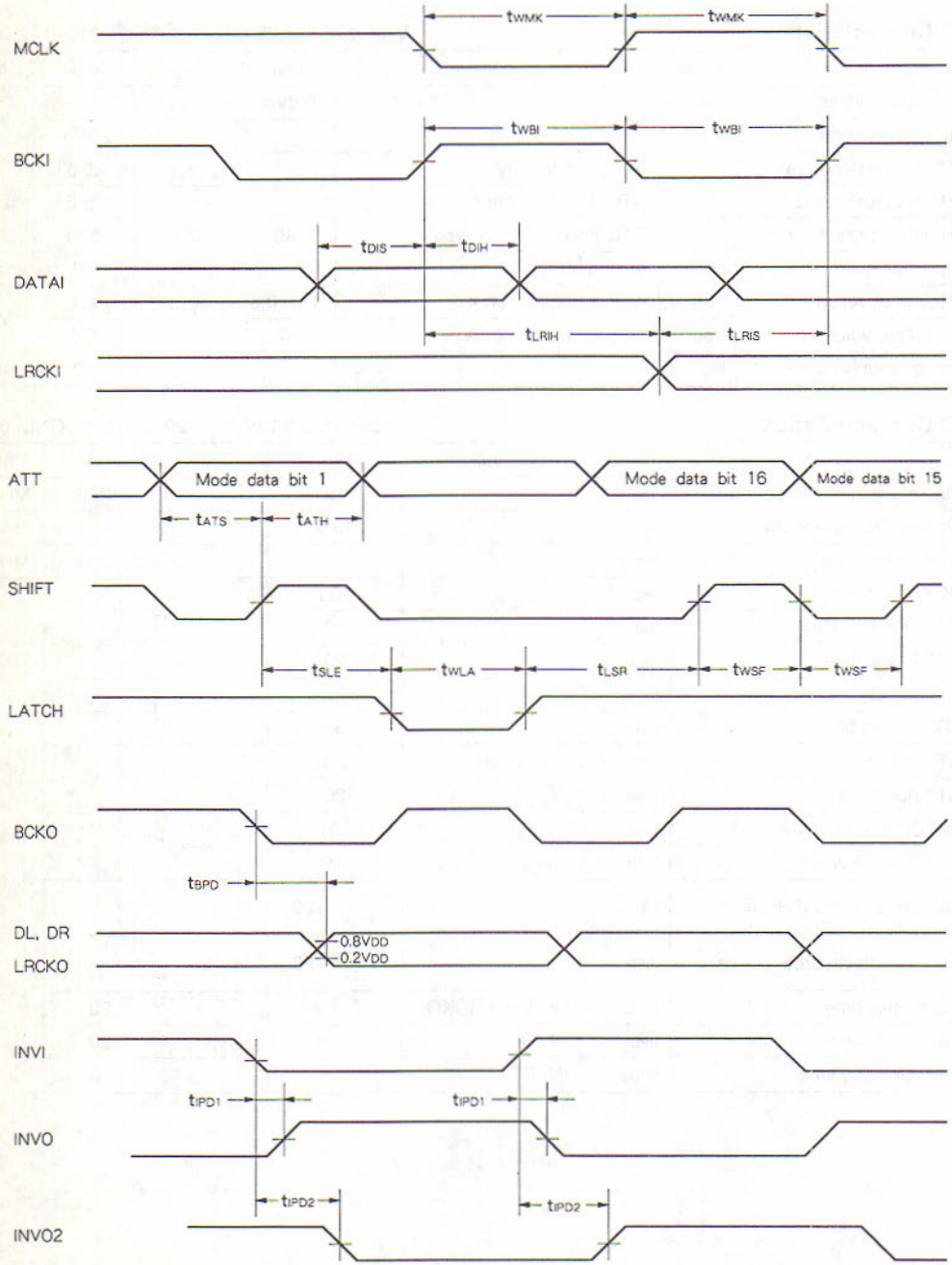
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	All inputs	0.8V_{DD}			V
"L" input voltage	V_{IL}				0.2V_{DD}	
"L" input leak current	I_{IL}	All inputs, V_{IN}=0V			± 5	μA
"H" input leak current	I_{IH}	CTL, all pins except 6, V_{IN}=V_{DD}			± 5	
"H" input current		CTL, pin 6 only, V_{IN}=V_{DD}	80	200	530	
Input capacitance	C_{IN}	All outputs		5	10	pF
"H" output voltage	V_{OH}	All outputs, Io=–2mA	V_{DD}–0.5		V_{DD}	V
"L" output voltage	V_{OL}	All outputs, Io=+2mA	0		0.4	
Power supply current	I_{DD}				60	mA

AC Characteristics

(V_{DD}=4.75 to 5.25V, Ta=–20 to +75 °C, GND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock input frequency	f_{MCLK}		15		27	MHz
Master CK pulse width	t_{WMK}		18.5			ns
BCKI frequency	f_{BCKI}				3.5	MHz
BCKI pulse width	t_{WBI}		100			ns
DATAI set-up time	t_{DIS}		20			
DATA hold time	t_{DIH}		20			
LRCKI set-up time	t_{LRIS}		50			
LRCKI hold time	t_{LRIH}		50			
ATT set-up time	t_{ATS}	CTL="L"	20			
ATT hold time	t_{ATH}		20			
LATCH effective time	t_{SLE}		0			
SHIFT pulse width	t_{WSF}		100			
LATCH "L" interval width	t_{WLA}		$\frac{4}{f_{MCLK}}$ +20			
SHIFT remover time	t_{LSR}		$\frac{8}{f_{MCLK}}$ +60			
Data delay time	t_{BPD}	DL, DR, LRCKO			20	
Inverter delay time	t_{IPD1}	INVO			20	
Inverter delay time	t_{IPD2}	INVO2			30	

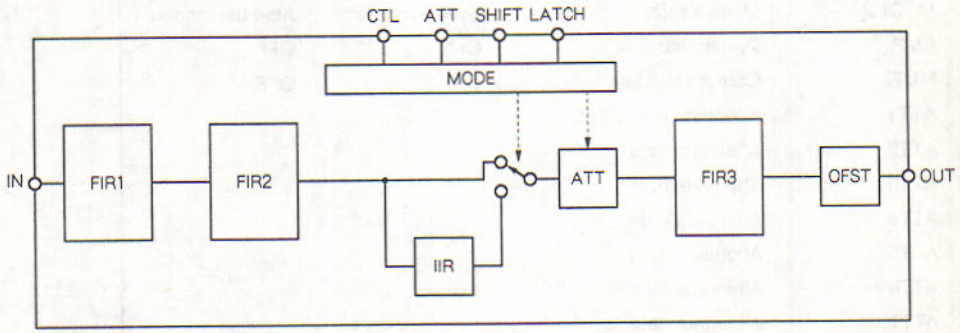
Input/Output Timing Chart (When no other specification threshold level is 0.5VDD)



Description of Functions

(1) Conceptual block chart

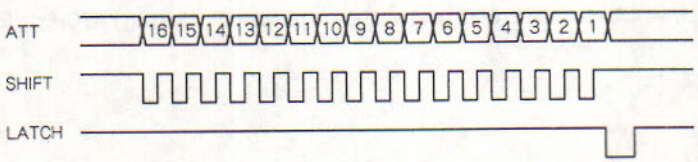
The conceptual block diagram for this LSI is shown below. Cascading of FIR1, 2, and 3 produces 8-times oversampling operation.



(2) Operating mode setting

The operation mode is set between ATT, SHIFT, or LATCH by transferring mode data. Mode data format is in the following format.

Bit-1 is always set to "0".



When bit-2 is "0" attenuate mode is set;
when set to "1" system mode is set.
When LATCH is "L" data cannot be transferred.

(3) Attenuate Mode

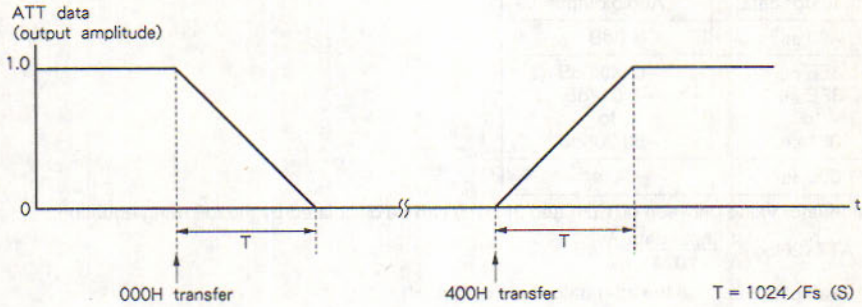
This mode is used to set either attenuate or de-emphasis mode.

	Mode flag	Function	"H"	"L"
1	MODE1	Mode switch	Test mode	Normal mode
2	MODE2	Mode switch	System mode	Attenuate mode
3	EMP	De-emphasis	ON	OFF
4	MUTE	Output zero data	ON	OFF
5	ATT1	Attenuate data (MSB)		
6	ATT2	Attenuate data		
7	ATT3	Attenuate data		
8	ATT4	Attenuate data		
9	ATT5	Attenuate data		
10	ATT6	Attenuate data		
11	ATT7	Attenuate data		
12	ATT8	Attenuate data		
13	ATT9	Attenuate data		
14	ATT10	Attenuate data		
15	ATT11	Attenuate data		
16	ATT12	Attenuate data (LSB)		

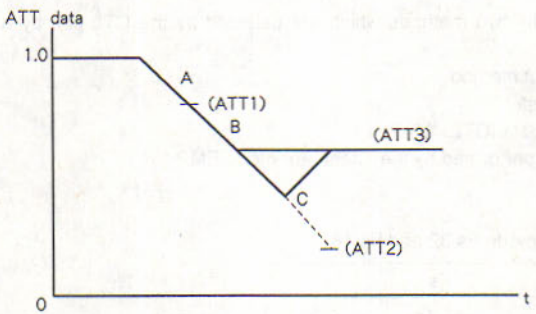
When the INIT pin is "L", MODE1, MODE2, EMP, and MUTE are re-set to "L". Setting LATCH pin to "L", enables the internal resistor.

① Attenuator

ATT data is a 12bits information transferred by bit-5 (MSB) through bit-16 (LSB). The size is 000H (0.0) to 400H (1.0). ATT data is set to 400H by INIT going "L".



The soft mute function is performed when ATT data is 000H. De-muting is performed by transferring 400H before the ATT data. (Chart above is for the case of 400H.)



Take the case of three attenuator data, ATT1, ATT2 and ATT3 and when their relations are ATT1 > ATT3 > ATT2. Assume that ATT1 is transferred first, followed by ATT2. If ATT2 is transferred before the ATT1 value is reached (during state A shown in the figure), attenuation directly approaches the value of ATT2. If ATT3 is transferred before the ATT2 value is attained (during state B or state C, the attenuation proceeds from the value attained at state B or state C to approach the value of ATT3. The transition from one attenuator datum to another is the same as in the case of soft muting.

ATT data= 400H System mode NS="High": Noise shaping OFF
System mode NS="Low": Noise shaping ON
≠400H case, noise shaping can operate whether or not NS is on or off.

Command input and audio output

Attenuator data consists of 12-bit, thus there are 1,024 various settings. The relationship between command and output is shown in the chart below.

Attenuator data	Audio output
400 (H)	0dB
3FF (H) 3FE (H) to 001 (H)	−0.0085dB −0.017dB to −60.206dB
000 (H)	$-\infty$

An attenuator value between 001 (H) and 3FF (H) can be calculated by the following equation.

$$ATT=20\log\left(\frac{\text{input data}}{1024}\right)\ dB$$

Example: Suppose the attenuator data is 3FA (H).

$$ATT=20\log\left(\frac{1018}{1024}\right)\ dB=-0.051dB$$

② De-emphasis

De-emphasis can be set by two methods which are selected by the CTL pin: by a serial transfer of mode data, or direct input pin.

CTL: "H": direct input method
"L": serial transfer

- Serial transfer of mode data (CTL: "L")

Emphasis ON/OFF is performed by the attenuator mode EMP

EMP: "H": ON
"L": OFF

Fs Selection System mode Fs 32 and Fs 48.

	Fs		
	32k	44.1k	48k
Fs32	H	L	L
Fs48	H	L	H

- Direct input (CTL: "H")

Emphasis ON/OFF is performed at the ATT pin.

ATT: "H": ON
"L": OFF

Fs Selection Performed at SHIFT, LATCH pin

	Fs		
	32k	44.1k	48k
SHIFT	H	L	L
LATCH	H	L	H

③ Mute

Output is muted when MUTE is raised "H". In this case the output is zero data.

(4) System mode

This mode sets the I/O data format, offset, and so forth.

	Mode flag	Function	"H"	"L"
1	MODE1	Mode switch	Test mode	Normal mode
2	MODE2	Mode switch	System mode	Attenuate mode
3	IFORM	Input data format	LSB first	MSB first
4	IBIT	Input data word length	18-bit	16-bit
5	OFORM	Output data format	LSB first	MSB first
6	OBIT	Output data word length	20-bit	18-bit
7	OFST	Append offset	ON	OFF
8	TEST1	Test mode setting	During normal use, fixed at "L"	
9	TEST2	Test mode setting	During normal use, fixed at "L"	
10	NS	Noise shaping	OFF	ON
11	MT1	Zero data detect time	60ms	300ms
12	MT2	Zero muting flag polarity	"H" sets mute	"L" sets mute
13	FS32	Selects de-emphasis Fs		
14	FS48			
15	SYNC	I/O synchronize		
16	STAT	Stop output clock		

	32K	44.1K	48K
FS32	H	L	L
FS48	H	L	H

When the INIT pin is "L", all the above are reset to "L".
Setting LATCH pin to "L", enables the internal resistor.

① Input data format
The input data format is set by IFORM.
IFORM: "H": LSB first
"L": MSB first

② Input data word length
The input data word length is set by IBIT.
IBIT: "H": 18-bit
"L": 16-bit

③ Output data format
The output data format is set by OFORM.
OFORM :"H": LSB first
"L": MSB first

④ Output data word length
The output data word length is set by OBIT
OBIT: "H": 20-bit
"L": 18-bit

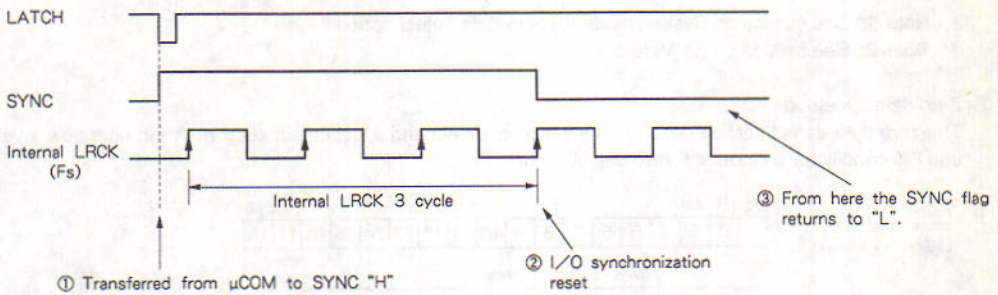
⑤ Offset
When OFST is raised "H", output data will have an offset value appended depending on how OBIT is set.
OBIT: "H": 02AAA (H)
"L": 02AA8 (H)

⑥ Zero data detect time
The input data's zero detect time is set by MT1. (Refer to the section on (5) zero detect functions for details.)
MT1: "H": 60ms
"L": 300ms

⑦ Zero muting flag polarity
The zero muting flag (FLGL, FLGR) polarity is set by MT2. (Refer to the section on (6) muting circuit functions for details.)
MT2: "H": zero mute flag is active when raised "H".
"L": zero mute flag is active when pulled "L".

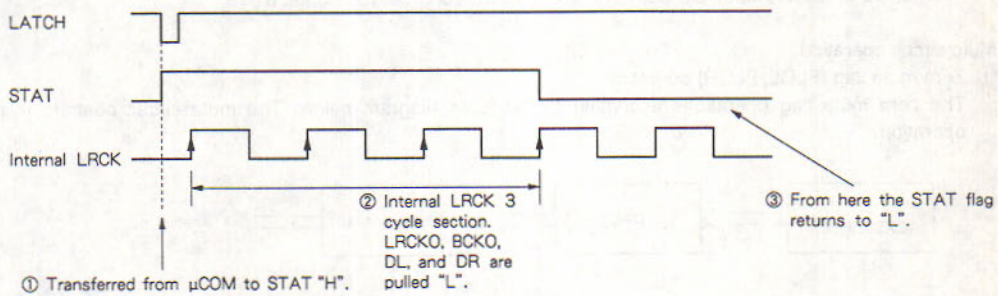
⑧ Input/Output synchronization
When SYNC goes "H", I/O synchronization is reset.

Example with SYNC flag raised "H".



⑨ Output clock stop
When the STAT signal is raised "H", the internal LRCK 3 cycle output clock (LRCKO, BCKO) and the output data (DL, DR) are pulled "L".

Example with STAT flag raised "H".



Mode settings are not limited to SYNC and STAT. Whether Attenuate mode or System mode is active, is determined by the final data transferred.

(5) Zero detect function

① Operation

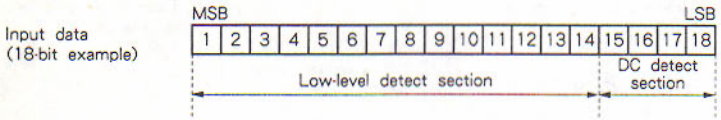
The input data controls the operation of zero detection and when continuing for zero data detect time *, zero mute flag (FLGL, FLGR) ** is active.

* Note 1: See section on System mode (6) zero data detect period.

** Note 2: See section on (6) Mute circuit control.

② Zero detect method

The zero data detect section consists of a low-level detect and a DC detect section. When both Low-level and DC conditions are present, zero detect occurs.



Zero data detect section structure

The low-level detect section senses whether the input data's first 14-bit are ALL0 or ALL1.
The DC detect section senses the input data doesn't change.

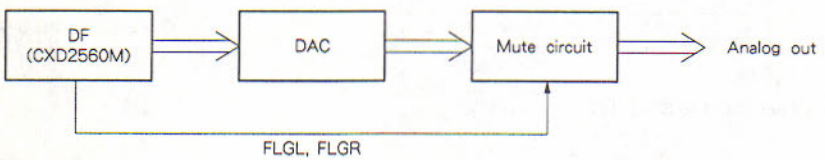
When 16-bit data is input, DC detection section consists of bit-15 and bit-16.

When 18-bit data is input, DC detection section consists of bit-15 through bit-18.

(6) Mute circuit operation

① Zero mute flag (FLGL, FLGR) operation

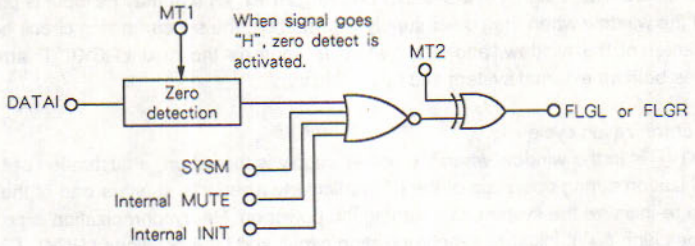
The zero mute flag operations according to the block diagram below. The mute circuit controls this operation.



Mute flag block diagram

② Zero muting flag construction

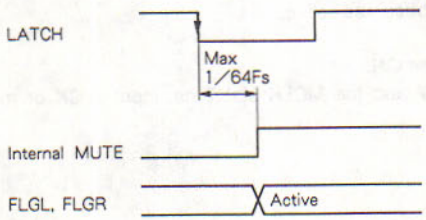
As shown in zero mute flag block diagram, zero mute flag is active by not only zero detect but also MUTE and INIT of system mute (SYSM) and attenuate mode.



Zero mute flag block diagram

③ Zero mute flag operation

- The zero mute flag is active during the zero detect cycle.
- When the SYSM signal goes "H", the zero mute flag is made active.
- When the MUTE ON function in Attenuate mode is used, the zero mute flag becomes active.

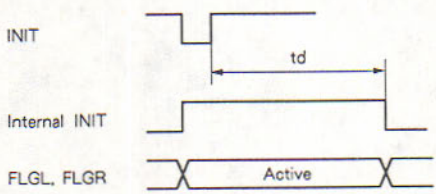


Zero mute flag output timing for the MUTE ON function.

(MUTE OFF operates in the same way.)

- INIT re-synchronization

The zero mute flag is active during INIT re-synchronization. When INIT is pulled "L" the zero mute flag is active. Also, after INIT is raised "H" (zero) the signal is held active for approximately 100 µs (Fs=44.1k).



$$\frac{4}{Fs} + \frac{1}{8Fs} < td < \frac{5}{Fs} + \frac{1}{8Fs}$$

Zero mute flag output timing for INIT re-synchronize cycle

(7) I/O synchronization circuit

① Theory of operation

The synchronizing circuit opens a window for eight internal system clocks (one clock=256Fs) to monitor whether the differentiated signal of the rise of LRCKI (LRCKI ⨍) that may be input is present. If the LRCKI ⨍ is out of the window when the power supply is turned on, the synchronizing circuit holds it at the time it is in the center of the window, and lets it start as soon as the next LRCKI ⨍ arrives. This process synchronizes both an external system and this LSI itself.

② INIT re-synchronization cycle

If the LRCKI ⨍ is in the window when the power supply is turned on, a fluctuation of LRCKI could cause re-synchronization during operation of the IC, particularly when it is at either end of the window. Thus it is important to re-initialize the system after turning the power on. Re-synchronization is performed at the time that INIT goes high (⨍), initialize synchronization circuit and then positions LRCKI ⨍ in the center of the window.

③ Operation when INIT is pulled "L".

Set input data to zero data.
Set output data to zero data.
Output clocks (LRCKO, BCKO, 128Fs) are continuously output.
Noise shaper register is cleared.
IIR register is cleared.
zero mute flag (FLGL, FLGR) becomes active.

④ Initialization process after power ON.

After V_{DD} reaches over 4.75V and the MCLK stabilizes, input 8 CK or more. Then bring INIT "H" to complete the initialization.

(8) I/O signal latch timing

① Input

ATT, SHIFT, LATCH: when INIT and CTL are pulled "H",
These input signals are latched to LRCKI by the appropriate internal clock .

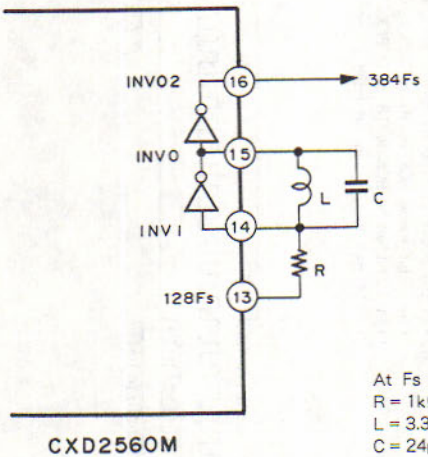
② Output

LRCKO, DL, DR:
These output signals are latched to BCKO by the appropriate internal clock.

(9) 384Fs oscillation synchronized by 128Fs

In CD applications utilizing DSP, it is possible to supply the master CK (384Fs).

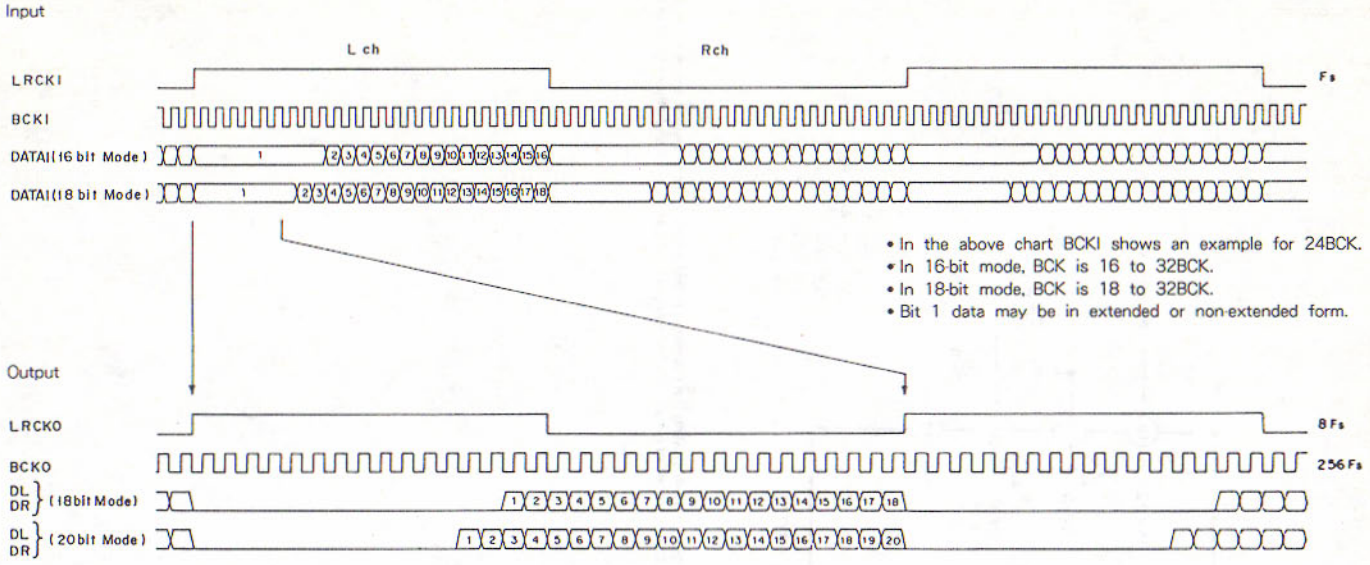
Application Circuit



At Fs = 44.1kHz,
R = 1kΩ
L = 3.3 µH
C = 24pF

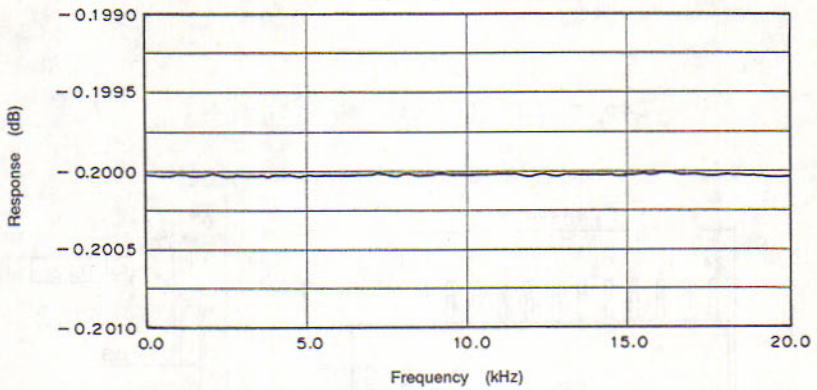
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

I/O Timing

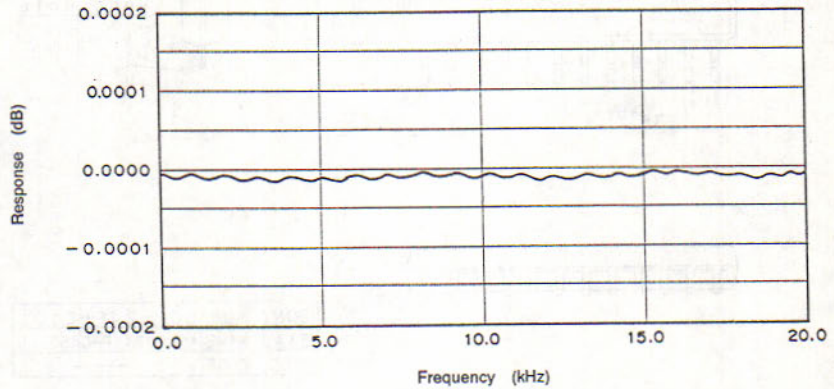

Input
L ch
Rch
LRCKI
Fs
BCKI
DATAI(16 bit Mode)
DATAI(18 bit Mode)
• In the above chart BCKI shows an example for 24BCK.
• In 16-bit mode, BCK is 16 to 32BCK.
• In 18-bit mode, BCK is 18 to 32BCK.
• Bit 1 data may be in extended or non-extended form.
Output
LRCKO
8Fs
BCKO
256Fs
DL
DR
(18bit Mode)
DL
DR
(20bit Mode)

Filter Characteristics (8Fs example)

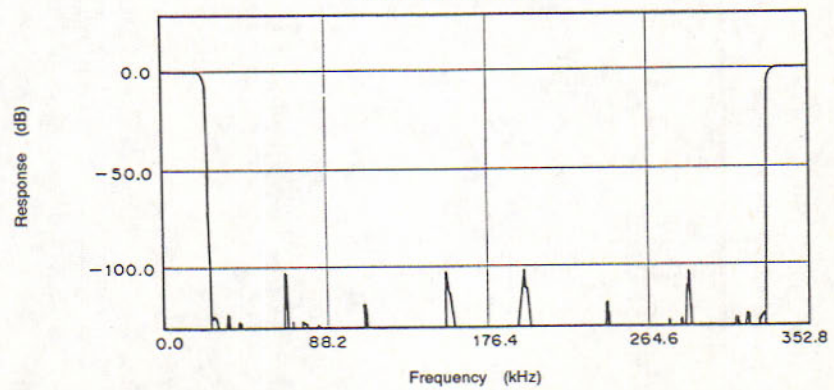
Frequency characteristics



Ripple characteristics

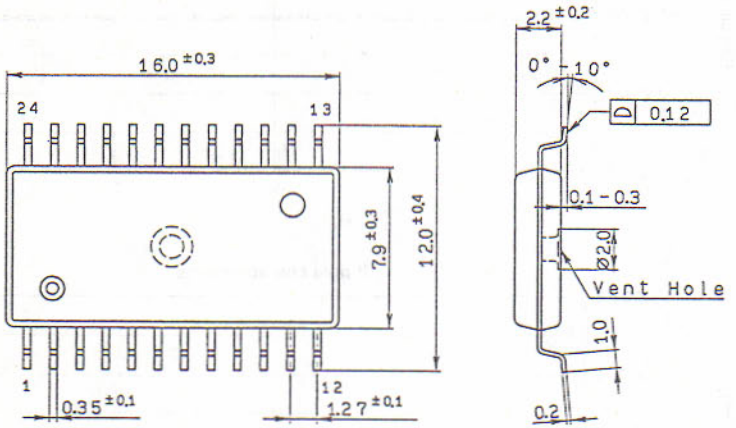


Attenuation characteristics



Package Outline Unit : mm

24pin SOP (Plastic) 450mil



SONY NAME	SOP-24P-L101
EIAJ NAME	*SOP024-P-0450-AU
JEDEC CODE	———

SONY

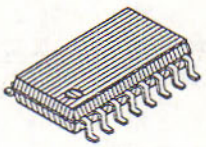
CXD2557M

Digital Audio Signal Silence Detector

Description

The CXD2557M is an LSI that detects silence in digital signals and outputs a muting signal if the silence continues for a fixed period of time.

16 pin SOP (Plastic)



Features

- Input format
  Two's complement MSB first
  16-bit serial data
  48 slots
- Silence detection time
  16,382 samples
- Silence detection level
  Upper 12 bits

Structure

Silicon gate CMOS IC

Application

Digital audio components

Absolute Maximum Ratings

• Supply voltage (see note)	V_{DD}	–0.5 to 7.0	V
• Input voltage	V_I	–0.5 to V_{DD}+0.5	V
• Output voltage	V_O	–0.5 to V_{DD}+0.5	V
• Input protection diode current	I_{IK}	–20 to 20	mA
• Output protection diode current	I_{OK}	–20 to 20	mA
• Output current	I_O	± 50	mA
• Package allowable power dissipation	P_D	0.8	W
• Storage temperature	Tstg	–65 to 150	°C

Note) Unless otherwise specified, voltage values are in reference to GND.

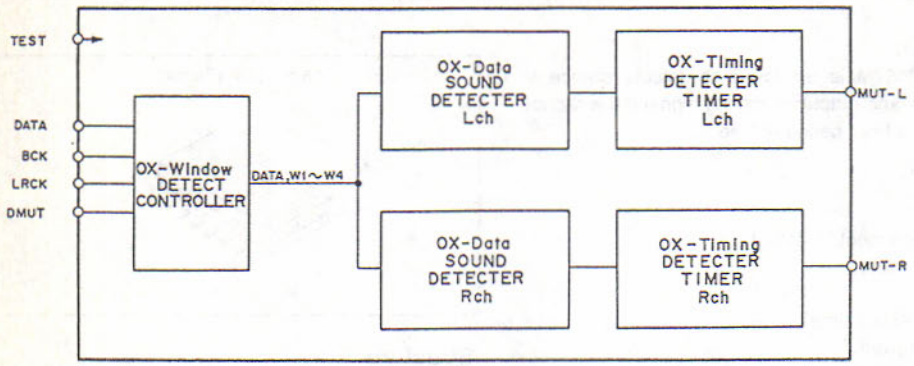
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (Typ. 5.0)	V
• High-level input voltage	V_{IH}	V_{DD} × 0.7 to V_{DD}	V
• Low-level input voltage	V_{IL}	GND to V_{DD} × 0.2	V
• Input rise and fall times (see note)	Tt	—— to 300	ns
• Operating temperature	T_A	0 to +70	°C

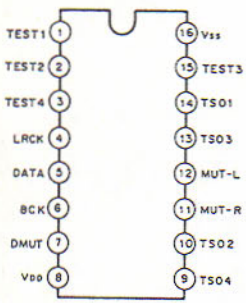
Note) Excluding schmitt trigger points.

E90823 – ST

Block Diagram and Pin Configuration (Top View)



W1 = All 0 or 1 DET bits Window, L : Active
W2 = 13~16bits Load Window, L : Active
W3 = OX and DIF DET Load Window, L : Active
W4 = MUT Timing Count Window, L : Active



Electrical Characteristics

(V_{DD}=5.0 ± 10%, T_A=0 to +70°C)

Item	Signal	Measurement conditions	Min.	Typ.	Max.	Unit
"H" output voltage	V_{OH}	I_{OH}=–4mA	3.7			V
"L" output voltage	V_{OL}	I_{OL}=4mA			0.4	V
Schmitt input hysteresis range	V_{T^+}–V_{T^-}		0.85		2.55	V
Input leakage current	I_{LI}	V_I=V_{DD} or GND			± 1	µA
Static current consumption	ICCq	V_I=V_{DD} or GND, all outputs open			+50	µA

Pin Description

Pin No.	Symbol	I/O	Description
1	TEST1	I	Test input. Normally set to "L".
2	TEST2	I	Test input. Normally set to "L".
3	TEST4	I	Test input. Normally set to "L".
4	LRCK	I	LR 2ch word clock (fs) signal. (48BCK=1 cycle)
5	SDATA	I	Serial data signal
6	BCK	I	Bit clock signal
7	DMUT	I	"H" forces MUT ON. "L" is set during normal operation.
8	V_{DD}	—	Power supply (+5 volts)
9	TSO4	O	Test output
10	TSO2	O	Test output
11	MUT-R	O	Rch MUT output
12	MUT-L	O	Lch MUT output
13	TSO3	O	Test output
14	TSO1	O	Test output
15	TEST3	I	Test input. Normally set to "L".
16	GND	—	0 volt

Description of Functions

1. System Configuration

This silence data detection IC is compatible with the data formats of the CDL-30, 35 and 40 series CD-use LSIs, and consists of a silence data detection circuit (0X-Data), a window generator (0X-Window), and a timer circuit (0X-Timer) which measures how long the silence continues.

2. Function and Operation of System Circuits

(1) Silence data detection circuit (0X-Data)

The silence data detection circuit is divided into two sections: a low-level detection circuit and a direct current detection circuit. Simultaneous detection of both the low-level state and direct-current state is treated as detection of silence data.

- Low-level detection circuit:

  Detects whether the absolute value of the signal is sufficiently small. Since the signal is two's complement data, the circuit checks whether the upper 12 bits are all 0's or all 1's.

- Direct current detection circuit:

  Detects whether the signal value changes. Since all bits up to bit 12 are either all 0's or all 1's, this circuit checks only bits 12 through 16 of each word for each channel. Also, for reading in data, both detection circuits use the no-change edge of the bit-clock data.

(2) Window generator (0X-Window)

The window generator generates the various latch pulses and load pulses necessary for the silence data detection and timer circuits.

- Window generator circuits:

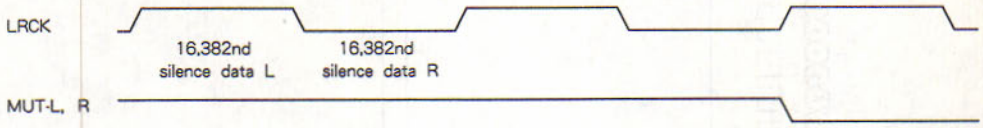
  These circuits generate the following windows and pulses: (1) W1 (Lch, Rch), a load window used by the low-level detection circuit; (2) W2 (Lch, Rch), a latch pulse used by the direct current detection circuit; (3) W3 (Lch, Rch), the silence data latch pulse; and (4) W4 (Lch, Rch) the timer count load pulse and MUT-T mute timing pulse.

(3) Timer circuit (0X-Timing)

This circuit checks whether the silence state continues for a time equivalent to 16,382 samples and outputs the muting signal.

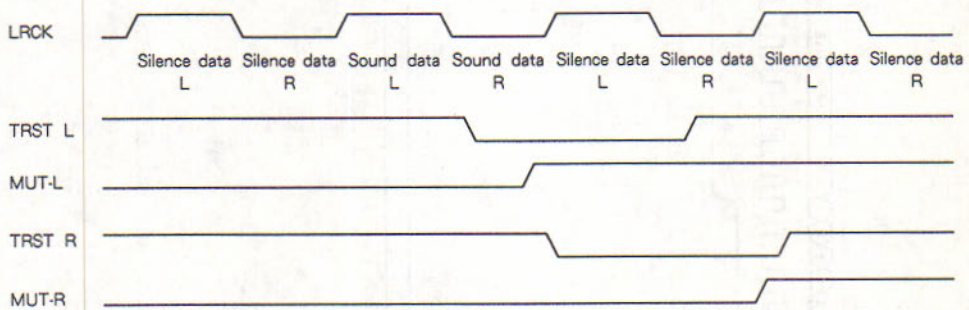
3. MUTE Output When Silence is Detected

If data judged as "silence" is input continuously for 16,382 cycles (16,382 fs cycles of LRCK), the mute signal is output ("L" level) on the rising edge of the second subsequent LRCK cycle.



The mute signal is reset as shown in the diagram below. If, for example, sound data is detected in the Lch signal, the internal TRST L signal goes to "L" on the rising edge of the fourth BCK cycle following the falling edge of LRCK, and the internal counter loads the initial value. As a result, the MUTE signal is reset on the rising edge on the next LRCK; the same occurs with the Rch signal.

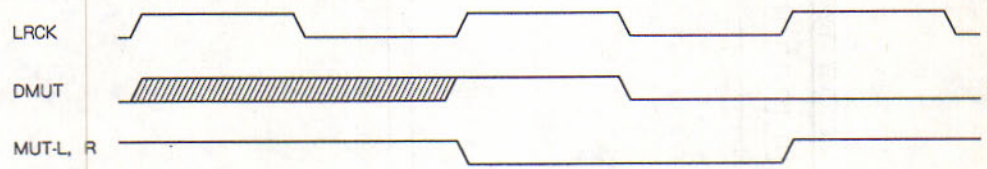
Note) The TRST L and R signals are flags showing whether the input data is silence or sound.
Silence: "H"; sound: "L".



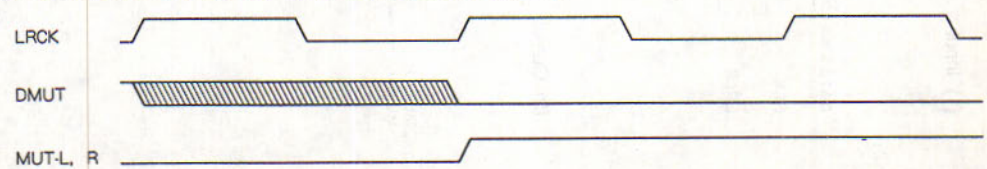
4. Forcing a MUTE Output Using the DMUT Input

When "H" is input to the DMUT pin, a MUTE signal is forcefully output to both L and R channels on the rising edge of the next LRCK. The MUTE signal is reset in the same manner.

1) When DMUT is turned ON while sound data is continuing:

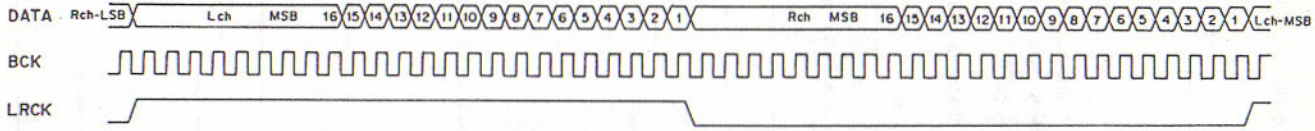


2) When DMUT is turned OFF while sound data is continuing:



Input/Output Timing

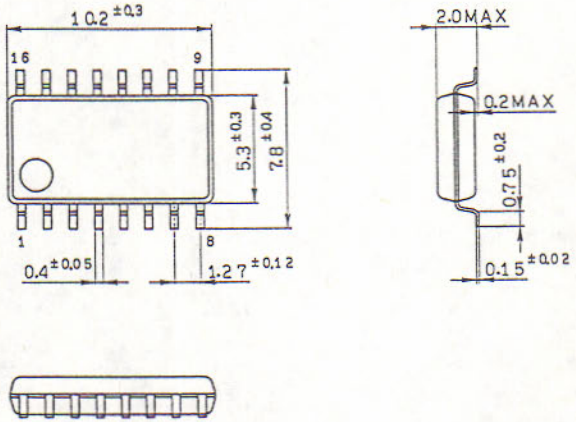
(1) Input



(2) Output

Package Outline Unit : mm

16pin SOP (Plastic) 300mil



SONY NAME	SOP-16P-L121
EIAJ NAME	*SOP016-P-0300-AX
JEDEC CODE	———

A/D, D/A Converter

2) A/D, D/A Converter

Type	Functions	Page
CXD2552Q	1-bit D/A converter	77
CXD2561BM	1-bit D/A converter, 3rd order noise shaper	85
CXD2555Q	1-bit A/D•D/A converter, Built-in digital filter, 2nd order noise shaper	94

SONY

CXD2552Q

1 Bit D/A Converter

Description

The CXD2552Q is 1 bit type D/A converter developed for digital audio products; compact disc player and others.

44 pin QFP (Plastic)

Features

- PLM pulse converter
- 3rd order noise shaper
- Direct digital sync
- Master clock 1024Fs
- 2 channel built in

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +6.5 V
- Input voltage V_I −0.3 to V_{DD}+0.3 V
- Allowable power dissipation
  P_D 500 mW (Ta=60°C)
- Storage temperature
  Tstg −55 to +150 °C

Structure

Silicon gate CMOS IC

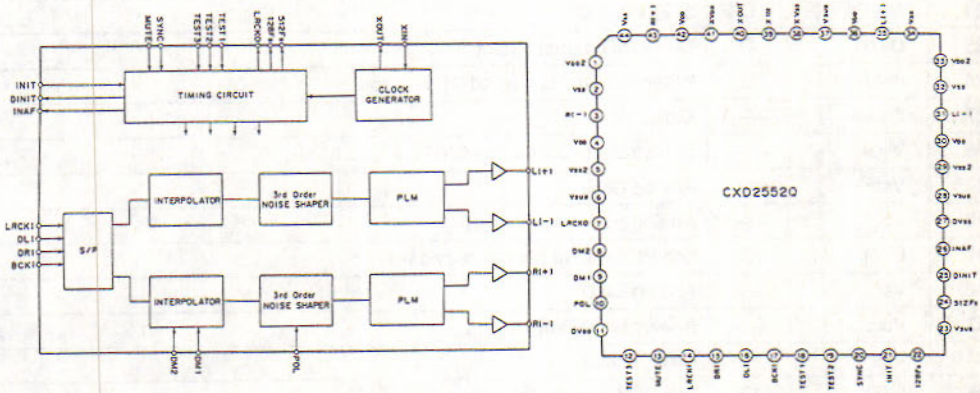
Applications

Compact disc player, digital amplifier, BS tuner

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25 V
- Operating temperature Topr −10 to 60 °C
- OSC frequency fx 32.0 to 49.7 MHz
- Supply voltage difference
  V_{DD}–V_{DD2}, V_{DD}–DV_{DD}, V_{DD}–XV_{DD} ± 0.1V
  V_{SS}–V_{SS2}, V_{SS}–DV_{SS}, V_{SS}–XV_{SS} ± 0.1V

Block Diagram and Pin Configuration



Sony Corporation developed CXD2552Q and designed the LSI circuitry that incorporates the Multi-Stage Noise Shaping technique originated by NTT (Nippon Telegraph and Telephone Corporation).

E89858A0Y – ST

Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD2}	—	Analog power supply
2	Vss	—	Analog GND
3	R (–)	O	Rch PLM output (Opposite phase)
4	V_{DD}	—	Analog power supply
5	V_{SS2}	—	Analog GND
6	V_{SUB}	—	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV_{DD}	—	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin.Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V_{SUB}	—	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DVss	—	Digital GND
28	V_{SUB}	—	Sub straight. Connect to GND.
29	V_{SS2}	—	Analog GND
30	V_{DD}	—	Analog power supply
31	L (–)	O	Lch PLM output (Opposite phase)
32	Vss	—	Analog GND
33	V_{DD2}	—	Analog power supply
34	Vss	—	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V_{DD}	—	Analog power supply
37	V_{SUB}	—	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	——	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XV_{DD}	——	Clock power supply
42	V_{DD}	——	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	Vss	——	Analog GND

Electrical Characteristics

DC Characteristics

($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60 °C)

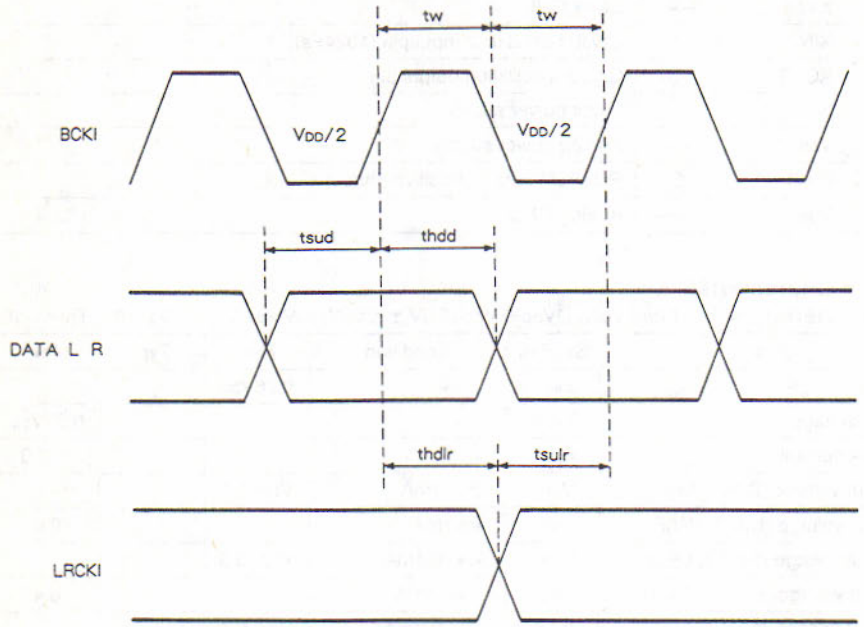
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	——	0.76V_{DD}			V
"L" input voltage	V_{IL}	——			0.24V_{DD}	V
Input leak current	I_{LI}	——			± 5.0	μA
"H" output voltage (DINIT, INAF)	V_{OH}	Io=−1mA	V_{DD}−0.5			V
"L" output voltage (DINIT, INAF)	V_{OL}	Io=1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V_{OH}	Io=−0.4mA	V_{DD}−0.5			V
"L" output voltage(512Fs, LRCKO)	V_{OL}	Io=0.4mA			0.4	V
"H" output voltage (128Fs)	V_{OH}	Io=−0.3mA	V_{DD}−0.5			V
"L" output voltage (128Fs)	V_{OL}	Io=0.3mA			0.4	V
"H" output voltage (R+, R−, L+, L−)	V_{OH}	Io=−15mA	V_{DD}−0.5			V
"L" output voltage (R+, R−, L+, L−)	V_{OL}	Io=15mA			0.5	V
"H" output voltage (XOUT)	V_{OH}	Io=−2.0mA	V_{DD}−0.5			V
"L" output voltage (XOUT)	V_{OL}	Io=2.0mA			0.4	V
Current consumption	I_{DD}	——		55	80	mA

AC Characteristics

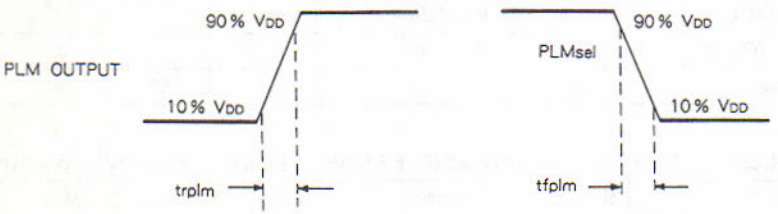
($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw		38			nsec
DATAL, R set up time	tsud		18			nsec
DATAL, R hold time	thdd		18			nsec
LRCKI set up time	tsulr		18			nsec
LRCKI hold time	thdlr		18			nsec
PLM output rise/fall time	tr, tf	CL=300pF		10		nsec

• **Input**



• **Output**



Analog Characteristics (V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V, V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	1kHz, 0dB/– ∞ dB data (Fs=44.1kHz) (A filte used)	96			dB

Electrical Characteristics Testing Method

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

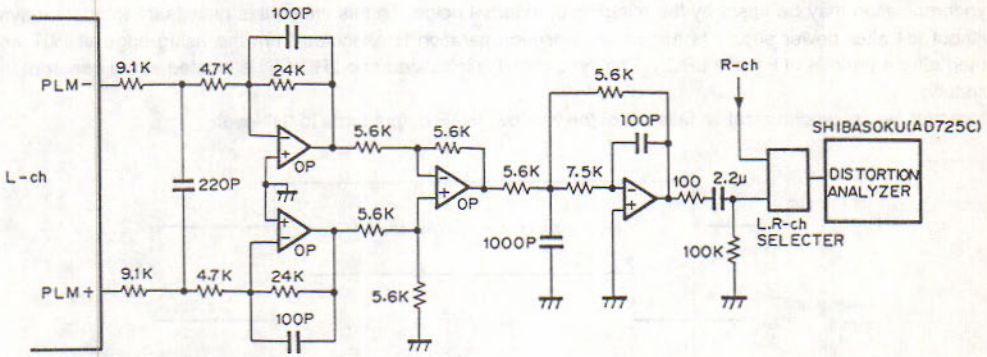


Fig. 1.

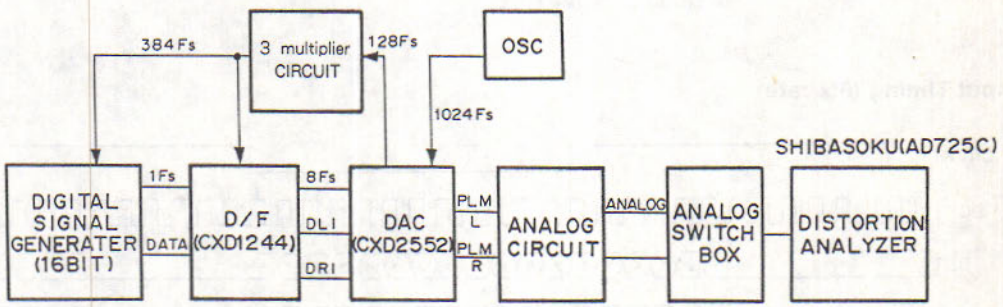


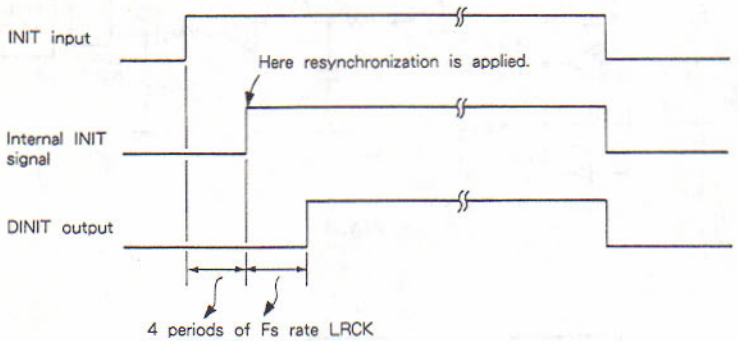
Fig. 2.

Description of Function

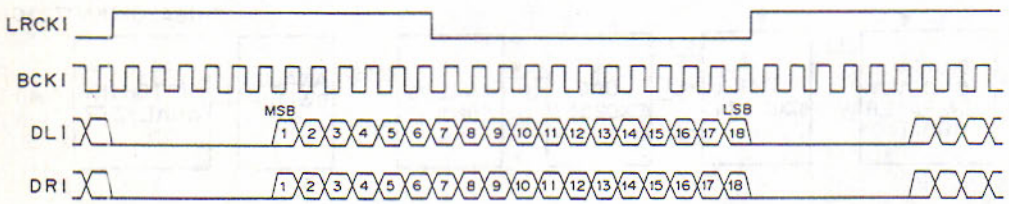
I/O Synchronizing Circuit

1) Theory of operation
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK ⌐) of the LRCK input has entered the window or not.
When power supply is turned on, should LRCK ⌐ be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK ⌐. Synchronization between the exterior system and this LSI is established through this operation.

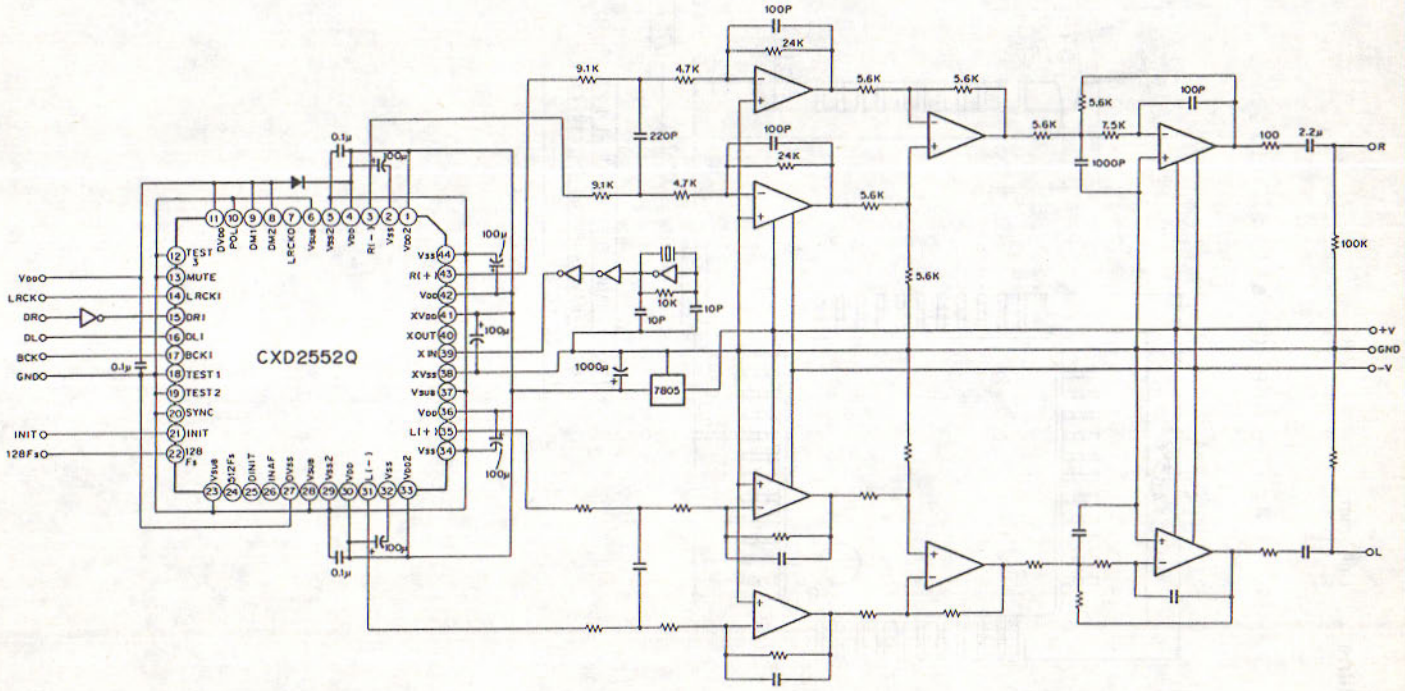
2) Resynchronization by means of INIT
Even when LRCK ⌐ is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK ⌐ is located at the center of the window.
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.



Input Timing (8fs rate)



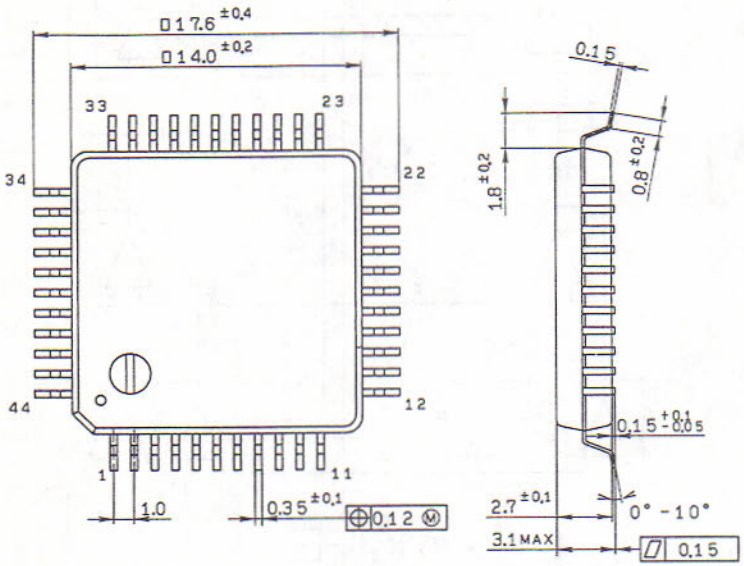
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	

SONY

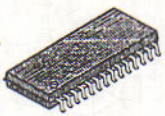
CXD2561BM

1-Bit D/A Converter for Audio Applications

Description

The CXD2561BM is a 1-bit stereo D/A converter using a 3rd-order noise shaper, in which DA conversion with superior characteristics can be achieved by employing an 8× oversampling digital filter. (By using two chips configuration, etc.)

28 pin SOP (Plastic)



Characteristics

- Distortion : 0.0035% and below
- S/N ratio : At least 95dB

Features

- 2-channel D/A converter on a single chip
- 3rd-order noise shaper
- PLM-method pulse conversion output
- Master clock of 512fs

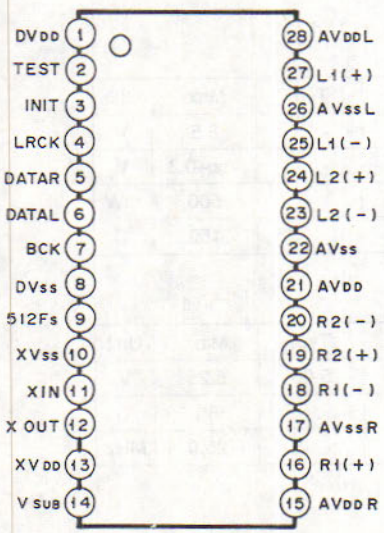
Structure

Silicon gate CMOS

Applications

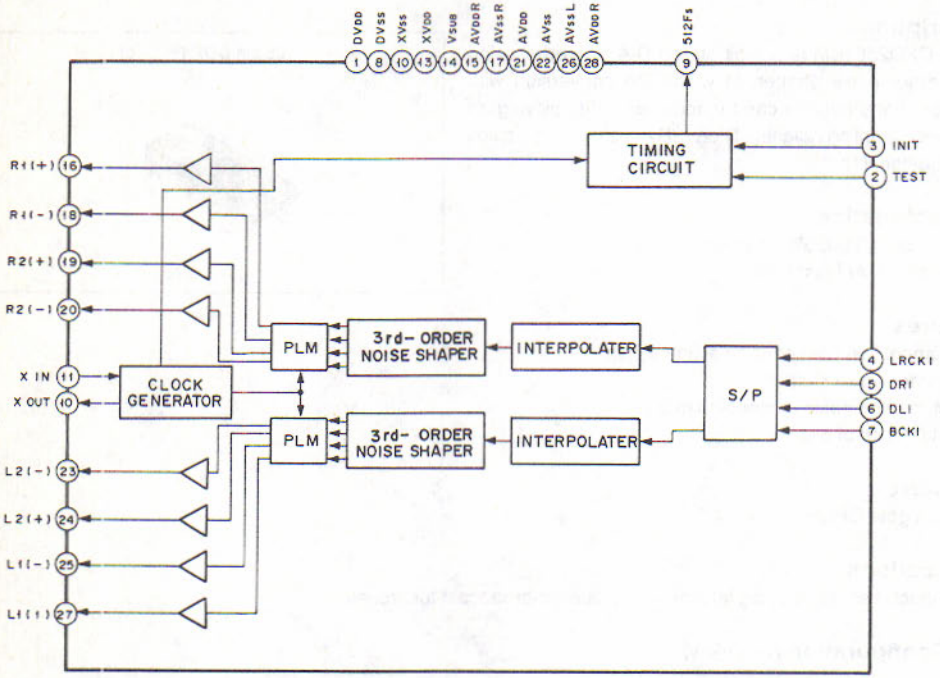
Compact-disc players, digital amplifiers, satellite-broadcast tuners, etc.

Pin Configuration (Top View)



E91Y36 – ST

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		−0.5		6.5	V
Input voltage	V_I		−0.3		V_{DD}+0.3	V
Allowable power dissipation	P_D	Ta=60 °C			500	mW
Storage temperature	Tstg		−55		150	°C

Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Operating temperature	Ta		−10		60	°C
OSC frequency	Fx	512fs	16.0		25.0	MHz

Pin Description

Pin No.	Symbol	I/O	Description
1	DV_{DD}	—	Digital power supply
2	TEST	I	Test pin. Fixed at "Low" in normal use.
3	INIT	I	Signal that activates resynchronization at rise
4	LRCK	I	LRCK input (8fs)
5	DATAR	I	Right channel data input (8fs); 16 to 18-bit data, LSB-first
6	DATAL	I	Left channel data input (8fs); 16 to 18-bit data, LSB-first
7	BCK	I	BCK input
8	DVss	—	Digital GND
9	512fs	O	512fs Clock output
10	XVss	—	Clock GND
11	XIN	I	Crystal oscillator input (512fs)
12	XOUT	O	Crystal oscillator output (512fs)
13	XV_{DD}	—	Clock power supply
14	Vsub	—	Connected to substrate GND
15	$AV_{DD}R$	—	Analog power supply for right channel
16	R1 (+)	O	Right-channel PLM output (in-phase)
17	AVssR	—	Analog GND for right channel
18	R1 (–)	O	Right-channel PLM output (opposite phase)
19	R2 (+)	O	Right-channel PLM output (in-phase)
20	R2 (–)	O	Right-channel PLM output (opposite phase)
21	AV_{DD}	—	Analog power supply
22	AVss	—	Analog GND
23	L2 (–)	O	Left-channel PLM output (opposite phase)
24	L2 (+)	O	Left-channel PLM output (in-phase)
25	L1 (–)	O	Left-channel PLM output (opposite phase)
26	AVssL	—	Analog GND for left channel
27	L1 (+)	O	Left-channel PLM output (in-phase)
28	$AV_{DD}L$	—	Analog power supply for left channel

Electrical Characteristics

DC Characteristics

(DV_{DD}=XV_{DD}=AV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V ± 5%, DV_{SS}=XV_{SS}=AV_{SS}=$AV_{SS}L$=$AV_{SS}R$=0V, Ta=−10 to 60°C)

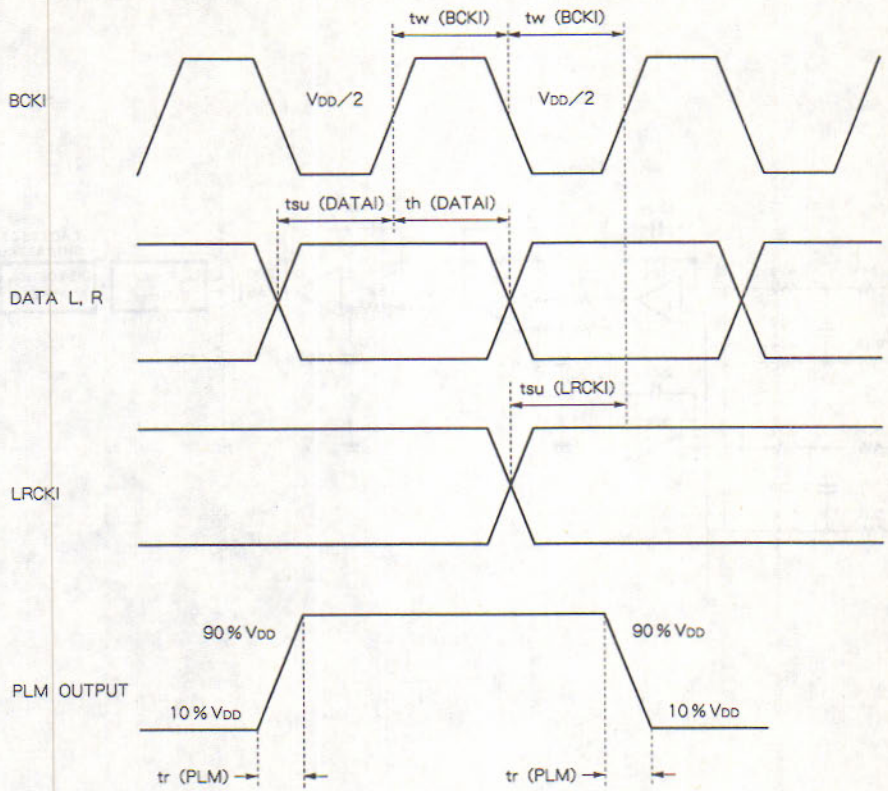
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
"High" level input voltage	XIN	V_{IH}		0.9V_{DD}			V
	Other pins	V_{IH}		0.76V_{DD}			V
"Low" level input voltage	XIN	V_{IL}				0.10V_{DD}	V
	Other pins	V_{IL}				0.24V_{DD}	V
Input leakage current		I_I		−5.0		5.0	μA
"High" level output voltage	512FS	V_{OH}	Io=−0.4mA	V_{DD}−0.5			V
	R (+/−), L (+/−)	V_{OH}	Io=−15mA	V_{DD}−0.5			V
	XOUT	V_{OH}	Io=−2.0mA	V_{DD}−0.5			V
"Low" level input voltage	512FS	V_{OL}	Io=0.4mA			0.4	V
	R (+/−), L (+/−)	V_{OL}	Io=15mA			0.5	V
	XOUT	V_{OL}	Io=2.0mA			0.4	V
Current consumption		I_{DD}			40	60	mA

AC Characteristics

(DV_{DD}=XV_{DD}=AV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V ± 5%, DV_{SS}=XV_{SS}=AV_{SS}=$AV_{SS}L$=$AV_{SS}R$=0V, Ta=−10 to 60°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	tw		38	40		nsec
DATAL, DATAR setup time	tsu		18	20		nsec
DATAL, DATAR hold time	th		18	20		nsec
LRCK setup time	tsu		18	20		nsec
PWM output rise time	tr	C_L=150pF		10		nsec
PWM output fall time	tf	C_L=150pF		10		nsec
XIN duty cycle	duty	V_{DD}/2 at 25MHz		50		%

Input/Output A/C Timing (8fs, data, BCK24 or BCK32)



Analog Characteristics

(DVDD=XVDD=AVDDR=AVDDL=5.0V ± 5%, DVss=XVss=AVss= AVssL=AVssR=0V, Ta=25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total harmonic distortion factor	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0035	%
S/N ratio	S/N	1kHz, 0/– ∞ 0dB data (Fs=44.1kHz)	95			dB

Electrical Characteristics Test Method

The total harmonic distortion factor and S/N ratio are tested by the circuits shown in Figures A and B.

Figure A

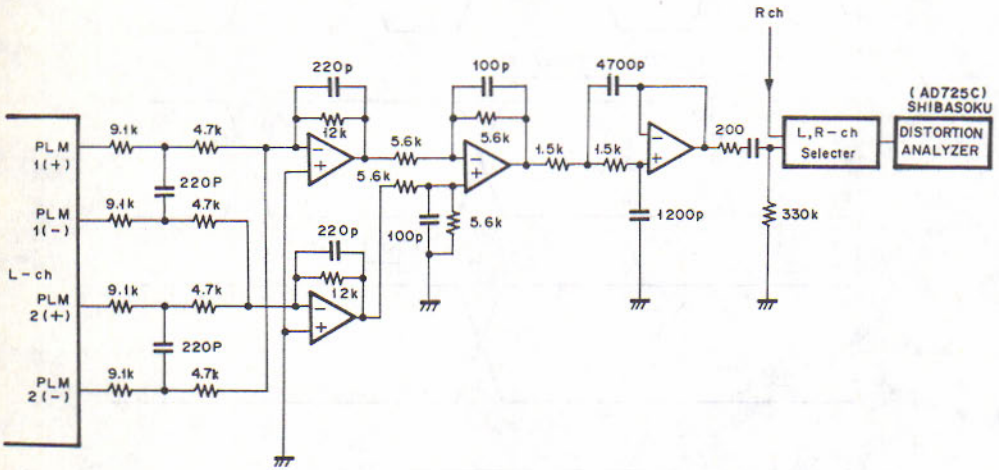
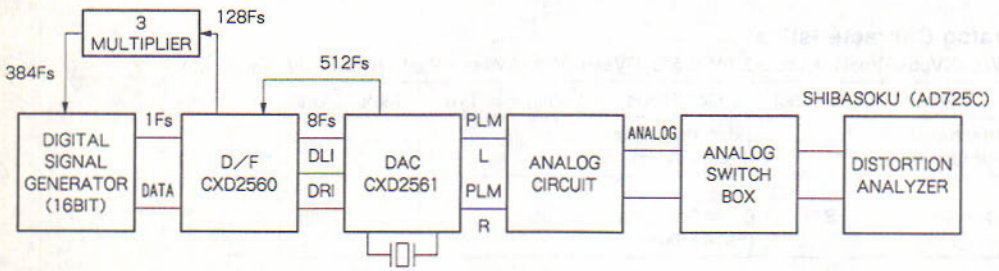


Figure B



Description of Functions

I/O Synchronization Circuit

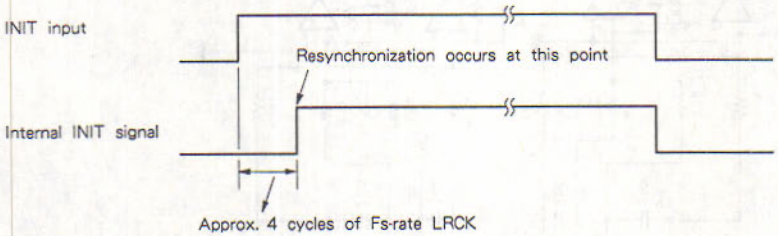
① Theory

The synchronizing circuit has a window for monitoring the input LRCK signal to determine whether there is a rising edge (LRCK ⌐) within it.

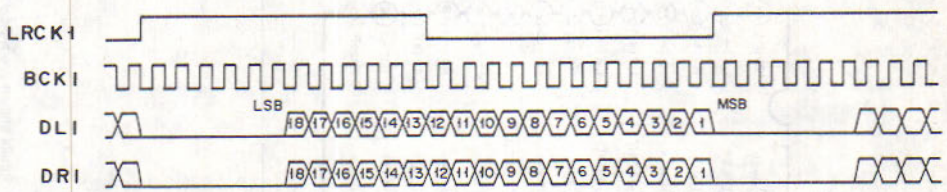
If the LRCK ⌐ is outside the window when power is switched on, the synchronizing circuit stops internal processing at timing centered on the window, and restarts in synchronization with the occurrence of the next LRCK ⌐. This operation synchronizes this LSI to external systems.

② Resynchronization by INIT

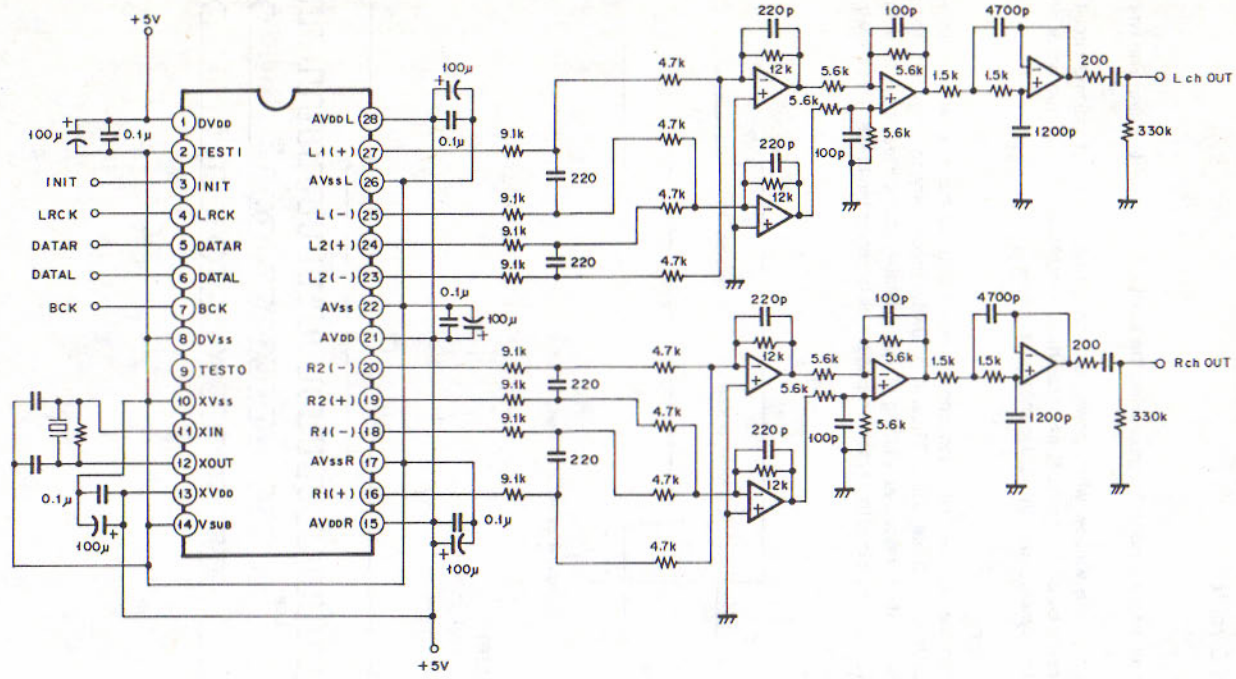
If the LRCK ⌐ is within the window, but is too close to either sides of the window, synchronization may be affected by factors such as external noise. Thus, it is always necessary to resynchronize after power is switched on. Resynchronization is done at a timing of approximately four cycles of LRCK at the Fs rate from the rising edge of INIT, and it initializes the synchronizing circuit to center the LRCK ⌐ in the window.



Input Timing (8fs Rate)



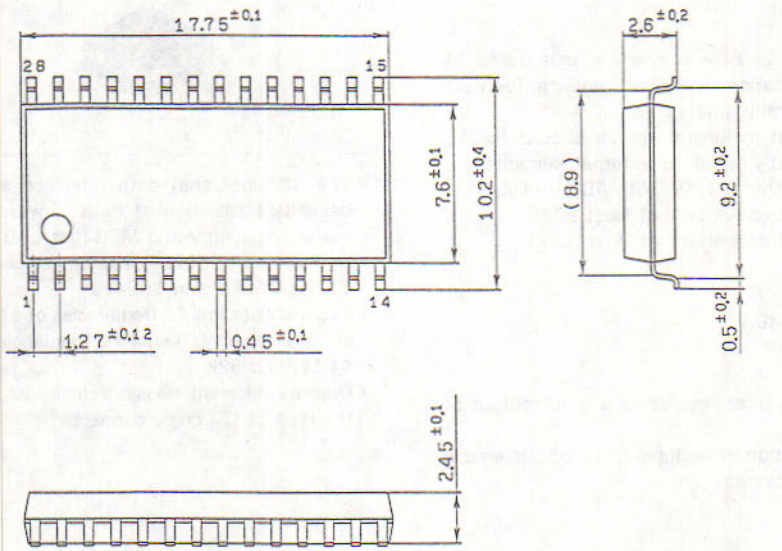
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

28pin SOP (Plastic) 375mil



SONY NAME	SOP-28P-L121
EIAJ NAME	*SOP028-P-0300-AX
JEDEC CODE	———

SONY

CXD2555Q

1Bit AD/DA Converter for Audio Application — Preliminary

Description

The CXD2555Q, which features a 2nd order ΔΣ noise shaper, is an extremely cost-effective 1-bit, 1-chip stereo AD/DA converter with on-chip digital filters.

48pin QFP (Plastic)

Features

- 2-channel AD and DA converters, plus digital filters for decimation and over-sampling for each converter, all on a single chip.
- Use of internal peripheral analog circuits for AD converter greatly simplifies external elements.
- Distortion: within 0.01% (both AD and DA)
- S/N ratio: DA converter: At least 90dB
  AD converter: At least 80dB

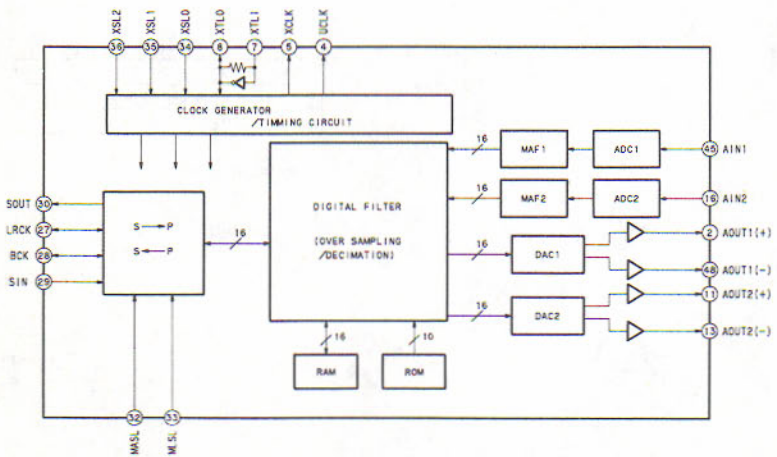
Structure

Silicon-gate CMOS

Functions

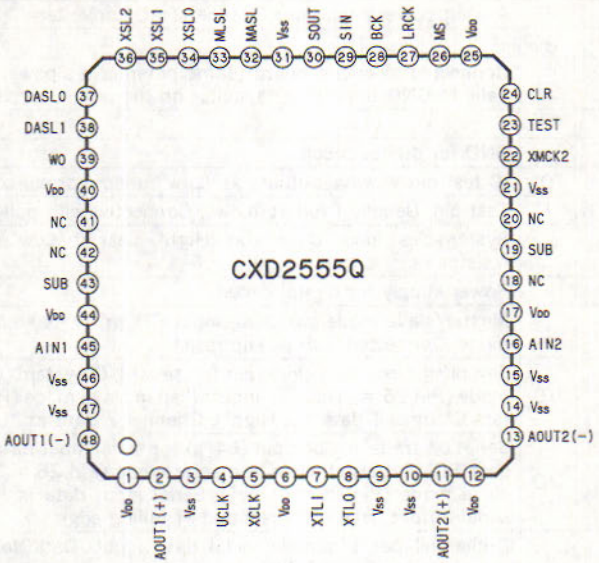
- On-chip digital filter enables data input/output at rate of 1×Fs
- Simple connection of multiple CXD2555Qs enable multi-channel system
- The 32 slot serial data interface enables independent selection of data forward-packing/rearward-packing and MSB-first/LSB-first.
- Applicable to four master clocks: 256Fs, 512Fs, 768Fs, and 1024Fs
- Applicable to low Fs frequencies of 16k, 8k and etc in addition to usual Fs frequencies of 48k, 44.1k, and 32k
- Outputs different division clocks according to the type of LSI chips connected

Block Diagram



PE91781-HP

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD}	—	Analog power supply for Channel 1 DA converter
2	AOUT1 (+)	O	Analog in-phase output for Channel 1 DA converter
3	V_{SS}	—	Analog GND for Channel 1 DA converter
4	UCLK	O	Output for 1/2 of clock frequency input through oscillator pin XTLI (Pin 7). User clock output for externally connected IC.
5	XCLK	O	Master clock output for ICs in slave mode, when the 256Fs clock output and more than one connections of CXD2555Qs are used. (XSL2 = "Low")
6	V_{DD}	—	Power supply for master clock
7	XTLI	I	Crystal oscillator circuit input. Connect the crystal oscillator selected by the crystal oscillator selection pins, XSL0 to XSL2 (Pins 34, 35, and 36). Input for external master clock
8	XTLO	O	Crystal oscillator circuit output. Connect the crystal oscillator selected by the crystal oscillator selection pins, XSL0 to XSL2 (Pins 34, 35, and 36).
9	V_{SS}	—	GND for master clock
10	V_{SS}	—	Analog GND for Channel 2 DA converter
11	AOUT2 (+)	O	Analog in-phase output for Channel 2 DA converter
12	V_{DD}	—	Analog power supply for Channel 2 DA converter
13	AOUT2 (−)	O	Analog opposite phase output for Channel 2 DA converter
14	V_{SS}	—	Analog GND for Channel 2 DA converter
15	V_{SS}	—	Analog GND for Channel 2 AD converter
16	AIN2	I	Analog input for Channel 2 AD converter

Pin No.	Symbol	I/O	Description
17	V_{DD}	—	Analog power supply for Channel 2 AD converter
18	NC	—	
19	SUB	—	Connected to circuit board (same potential as power supply) within the IC. Falls to GND through a capacitor on the printed circuit board.
20	NC	—	
21	V_{SS}	—	GND for digital circuits
22	XMCK2	O	IC test pin. Always outputs at "Low" under normal conditions.
23	TEST	I	Test pin. Usually fixed at "Low". Connected with pull-down resistor.
24	CLR	I	System-clear input. Usually at "High". clear at "Low". Connected with pull-up resistor.
25	V_{DD}	—	Power supply for digital circuits
26	MS	I	Master/slave mode switching input. "High" = master mode; "Low" = slave mode. Connected with pull-up resistor.
27	LRCK	I/O	Sampling frequency clock pin for serial I/O system. Output when in master mode (Pin 26 = "High"); input when in slave mode (Pin 26 = "Low"). Transfers Channel 1 data at "High"; Channel 2 data at "Low".
28	BCK	I/O	Serial bit transfer clock pin (64Fs) for serial input data SIN and serial output data SOUT. Output when in master mode (Pin 26 = "High"); input when in slave mode (Pin 26 = "Low"). Serial input data is fetched at rising edge; serial output data is transmitted at falling edge.
29	SIN	I	2-channel per 1 sample serial data input. Data format is based on the complement of 2; 32-bit slot.
30	SOUT	O	2-channel per 1 sample serial data output. Data format is based on the complement of 2; 32-bit slot.
31	V_{SS}	—	GND for digital circuits.
32	MASL	I	For serial I/O with 16-bit serial data, selects either the first 16-bit slot or the last 16-bit slot of the 32-bit slot. "High" means forward packing; "low" means rearward packing.
33	MLSL	I	With serial I/O, selects either LSB-first or MSB-first for input/output to put in 16-bit serial data. "High" = MSB-first; "Low" = LSB-first.
34	XLS0	I	Crystal selection pin. Use 3-bit, XSL0 to XSL2, to select the clock input frequency from XTLI (Pin 7).
35	XSL1	I	
36	XSL2	I	
37	DASL0	I	IC test pin. Normally fixed at "High".
38	DASL1	I	IC test pin. Normally fixed at "Low".
39	WO	I	Synchronization window open input. "High" = window masked; "Low" = window open (forced synchronization). Connected with pull-up resistor.
40	V_{DD}	—	Power supply for digital circuits.
41	NC	—	
42	NC	—	
43	SUB	—	Connected to a circuit board (same potential as power supply) within the IC. Falls to GND through a capacitor on the printed circuit board.
44	V_{DD}	—	Analog power supply for Channel 1 AD converter
45	AIN1	I	Analog input for Channel 1 AD converter
46	V_{SS}	—	Analog GND for Channel 1 AD converter
47	V_{SS}	—	Analog GND for Channel 1 DA converter
48	AOUT1 (−)		Analog opposite phase output for Channel 1 DA converter

Electrical Characteristics

Absolute Maximum Ratings (T_a = 25°C, V_{SS} = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.5\sim7.0$	V
Input voltage	V_I	$V_{SS}-0.5\sim V_{DD}+0.5$	V
Output voltage	V_O	$V_{SS}-0.5\sim V_{DD}+0.5$	V
Operating temperature	T_{opr}	$-20\sim+75$	°C
Storage temperature	T_{stg}	$-55\sim+150$	°C

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Operating temperature	T_a	−20		+75	°C
Sampling frequency	F_S	—		—	kHz

(Note) The analog power supply (Pins 17 and 44) must be turned on at either the same time or before the power sources. Turning this power on after the other power sources may cause latch-up. There are no specific limitations on the order in which power supplies are turned off.

Input/Output Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
Bi-directional pin	$C_{I/O}$			11	pF

Test conditions: V_{DD} = V_I = 0V, f = 1MHz

DC Characteristics

Item	Symbol	Condition	Min.	Max.	Unit	Applicable pin
Input voltage	V_{IH}		$0.7V_{DD}$		V	* 1
	V_{IL}			$0.3V_{DD}$		
	V_{IN}	Analog input	V_{SS}	V_{DD}	V	* 2
Output voltage	V_{OH}	$I_{OH}=2mA$	$V_{DD}-0.5$	V_{DD}	V	* 3
	V_{OL}	$I_{OL}=4mA$	0	0.4		
	V_{OH}	$I_{OH}=-4mA$	$V_{DD}-0.5$	V_{DD}	V	* 4
	V_{OL}	$I_{OL}=4mA$	0	0.4		
	V_{OH}	$I_{OH}=-12mA$	$V_{DD}/2$	V_{DD}	V	* 5
	V_{OL}	$I_{OL}=16mA$	0	$V_{DD}/2$		
	V_{OH}	$I_{OH}=-2mA$	$V_{DD}-0.8$	V_{DD}	V	* 6
	V_{OL}	$I_{OL}=imA$	0	0.4		
Input leakage current (1)	I_{LI1}		−10	10	μA	* 7
Input leakage current (2)	I_{LI2}		−40	40	μA	* 8
Output leakage current	I_{SS}		−40	40	μA	* 9
Feedback resistance	R_{LZ}	V_{IN} = V_{SS} or V_{DD}	250k	2.5M	Ω	* 10

* 1 During input to all input pins except AIN1 and AIN2, and bi-directional pins (BCK and LRCK)
* 2 AIN1 and AIN2
* 3 XCLK, XMCK2, and SOUT
* 4 AOUT1 (+), AOUT1 (−), AOUT2 (+), AOUT2 (−), and UCLK
* 5 XTLO
* 6 During output from bi-directional pins (BCK and LRCK)
* 7 All input pins except AIN1 and AIN2
* 8 During input to bi-directional pins (BCK and LRCK)
* 9 SOUT, AOUT1 (+), AOUT1 (−), AOUT2 (+), AOUT2 (−), and UCLK
* 10 Resistance between XTLO and XTLI (reference value = 1MΩ)

Description of Functions

① Serial data interface

[Related pins] LRCK, BCK, SOUT, SIN, MASL, MLSL

The serial data format is the same for both SIN (DA converter input) and SOUT (AD converter output); it is 2-channel per 1 sample serial data based on the complement of 2. Each channel is divided into 32-bit slots of which 16 bits are handled as data.

Within the 32-bit slot, valid data can be selected independently by MASL to be either the first 16-bit or the last 16-bit.

The serial data arrangement can also be selected independently by MLSL to be either MSB-first or LSB-first.

MASL	
High	Forward packing
Low	Rearward packing

MLSL	
High	MSB-first
Low	LSB-first

② Master mode/slave mode

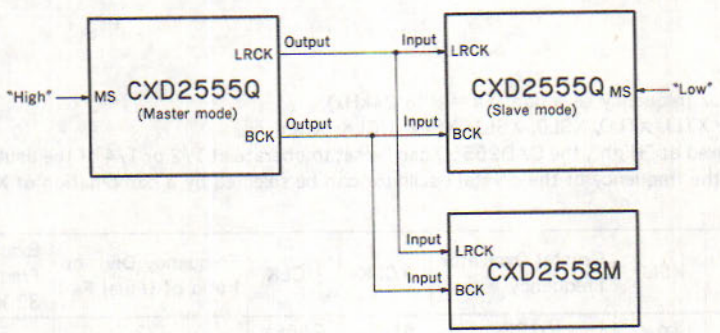
[Related pins] MS, LRCK, BCK

When either connecting several CXD2555Qs together or pairing one CXD2555Q with a CXD2558M, put one of the CXD2555Qs in use to master mode to act as the supply source to LRCK and BCK.

The other CXD2555Qs are used in slave mode to receive data from the master through LRCK and BCK.

MS	Mode	LRCK and BCK I/O
High	Master mode	Output
Low	Slave mode	Input

[Connection example]



③ Crystal oscillator frequency selection (Fs = 32 to 48kHz)

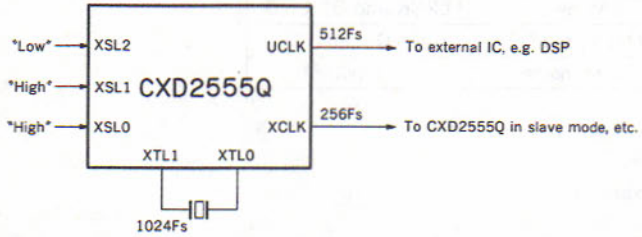
[Related pins] XTLI, XTLO, XSL0, XSL1, XSL2, UCLK, XCLK

The frequency of a crystal oscillator connected externally to XTLI and XTLO can be selected by fixing XSL2 at "Low" and combining XSL0 and XSL1 settings. In this case, the output from XCLK is always 256 times the amount of Fs, and the clock output from UCLK is 1/2 the crystal oscillator frequency.

Note that if input is to be done by an external master clock and not a crystal oscillator, input will be through XTLI and XTLO should be left open.

XSL2	XSL1	XSL0	Crystal Oscillator Frequency	XCLK	UCLK
Low	Low	Low	256Fs	256Fs	128Fs
Low	Low	High	512Fs	256Fs	256Fs
Low	High	Low	768Fs	256Fs	384Fs
Low	High	High	1024Fs	256Fs	512Fs

[Selection example]



④ Crystal oscillator frequency selection (Fs = 8 to 24kHz)

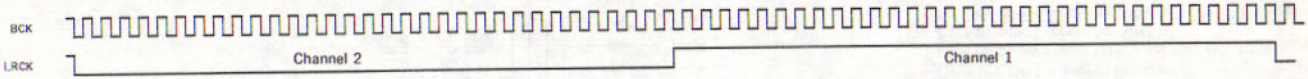
[Related pins] XTLI, XTLO, XSL0, XSL1, XSL2, UCLK, XCLK

When XSL2 is fixed at "High", the CXD2555Q can be set to operate at 1/2 or 1/4 of the usual Fs frequency. In this case also, the frequency of the crystal oscillator can be selected by a combination of XSL0 and XSL1 settings.

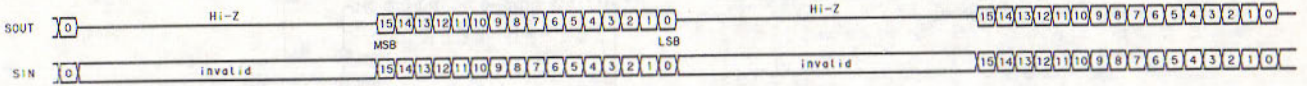
XSL2	XSL1	XSL0	Crystal Oscillator Frequency *	XCLK	UCLK	Frequency Division Ratio of Usual Fs	Example at Usual Frequency of 32 kHz
High	Low	Low	512Fs	512Fs	256Fs	1/2	Fs=16kHz
High	Low	High	1024Fs	1024Fs	512Fs	1/4	Fs=8kHz
High	High	Low	1024Fs	512Fs	512Fs	1/2	Fs=16kHz
High	High	High	2048Fs	1024Fs	1024Fs	1/4	Fs=8kHz

* If the usual frequency is 32 kHz, its value at 1/2 and 1/4 would be 16kHz and 8kHz respectively. Given the same calculations, the low Fs frequencies of 44.1kHz and 48kHz are 22.05kHz/11.025kHz and 24kHz/12kHz respectively.

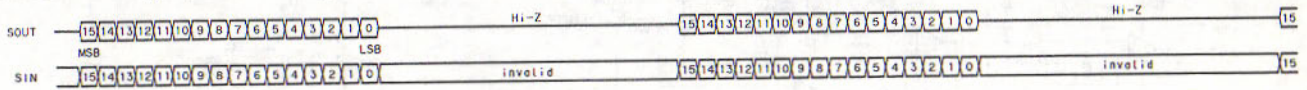
Serial Data Interface Timing



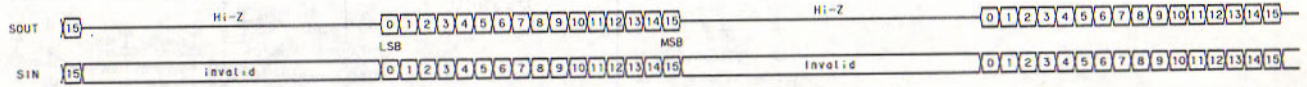
MLSL = "High" , MASL = "Low"



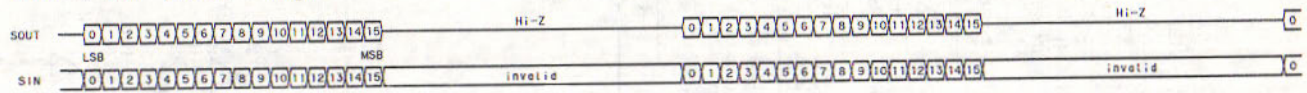
MLSL = = "High" , MASL = "High"



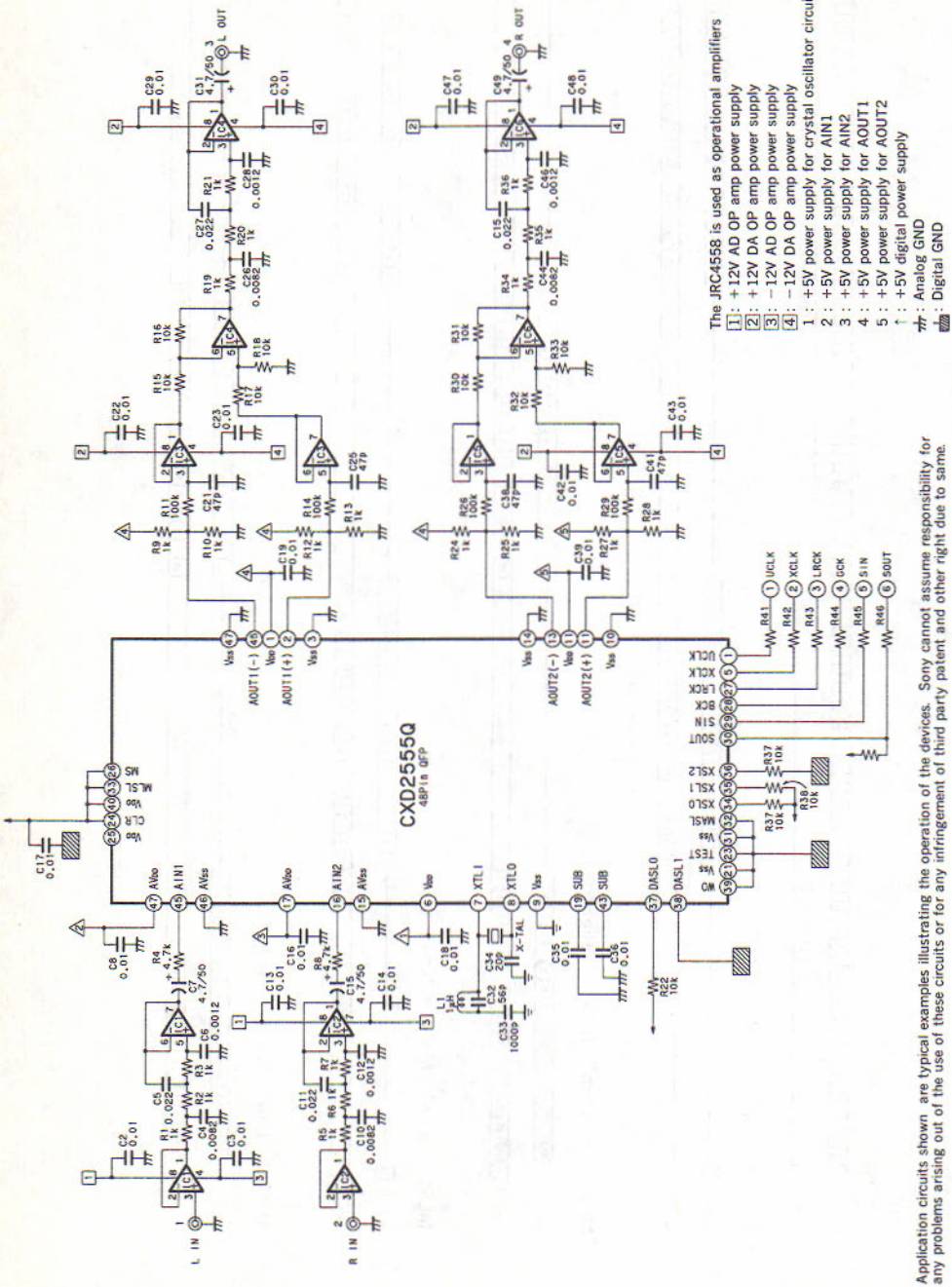
MLSL = "Low" , MASL = "Low"



MLSL = "Low" , MASL = "High"



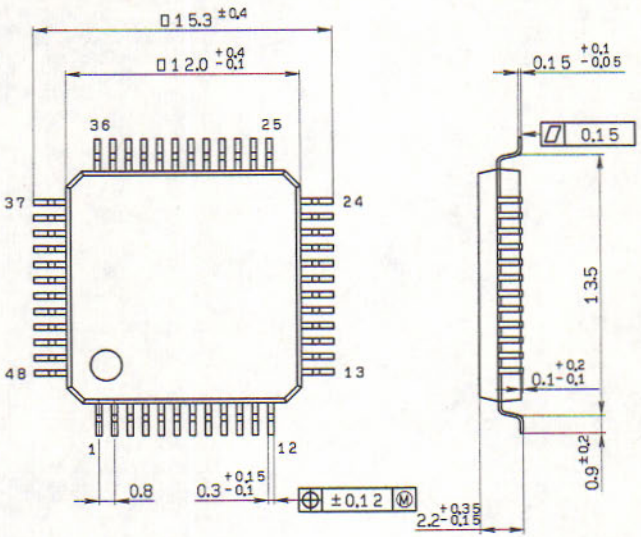
Application Circuit Master mode (MS = "High")



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	•QFP048-P-1212-B
JEDEC CODE	———

ADSP
(Audio Digital Signal Processor)

3) ADSP (Audio Digital Signal Processor)

Type	Functions	Page
CXD1160AP CXD1160AQ	Software realized various digital audio data. Double accuracy arithmetic possible	107
CXD1355AQ	Programmable DSP and 8fs over sampling digital filter for surround	159
CXD2701Q	Programmable DSP+Equalizer for surround Characteristics realized by fixing algorithm at equalizer and giving coefficient from exterior	179

SONY®

CXD1160AP/AQ

Digital Audio signal processing LSI

Description

CXD1160AP/AQ is a digital audio signal processing LSI.

Features

This LSI features built-in instruction RAM, coefficient RAM, multiplier, barrel shifter and others. With regards to peripheral interface usage, serial I/O, delay I/O (stereo delay for a max. of 1024 samples possible) and microcomputer interface provide excellent system cost performance.

Structure

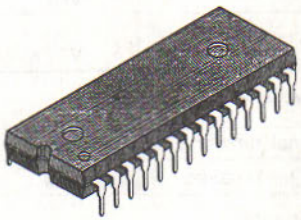
Silicon gate CMOS

Functions

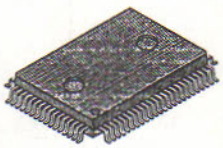
(1) Hardware

• Master clock	30.72MHz max. (during MCK1 input) 15.36MHz max. (during MCK2 input)
• Machine cycle	130ns min. (160 cycle max./fs=48KHz)
• Instruction	1 to 3 cycle (single precision/ double precision)
• Built-in RAM	Instruction RAM 24bit×64w coefficient RAM 16bit×64w data RAM 16bit×64w
• Multiplying part	16bit×16bit built-in multiplier data coefficient (1) 16×16 (1 cycle) (2) 16×32 (2 cycle) (3) 32×16 (2 cycle) (4) 32×32 (3 cycle)
• Adder-Subtractor	34bit±34bit Acc 34bit with 2bit shifter
• Register	For adder-subtractor R (H/L) Serial I/O I 1 (H/L) I 2 (H/L) O 1 (H /L) O 2 (H/L) Delay I/O D1 (H/L) D 0 (H/L) Every register 32bit H/L can be used independently

CXD1160AP 28pin DIP (Plastic)



CXD1160AQ 80pin QFP (Plastic)



• Barrel shifter	Positive floating point Type conversion Arithmetic left shift Arithmetic right shift 32bit IN 16bit OUT shift max. 15bit
• Address stack	double
• Loop counter	4bit

(2) Interface

• Serial I/O	Time-shared 2ch input 2ch output Every channel data format 32bit, (16bit+16bit), 24bit, 16bit, Every channel bit clock format 32ck, 24ck MSB first
• Delay I/O	Every channel variable delay (1 to 1024 samples) Usage also possible as serial I/O
• Microcomputer interface	

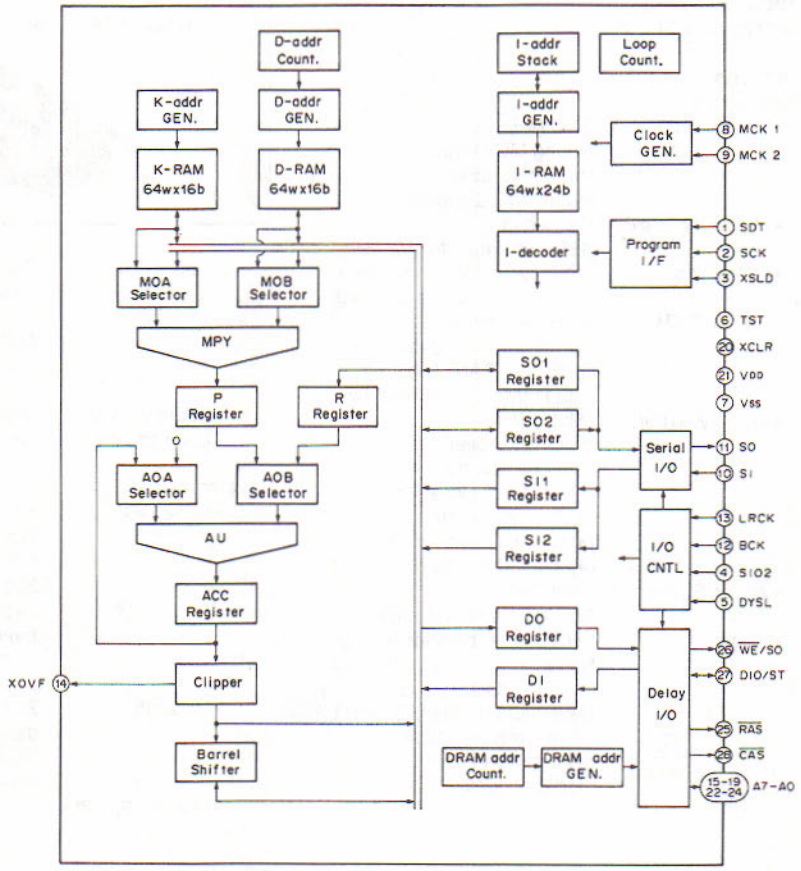
E88Z02A15-YA

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings		Unit
		Min.	Max.	
Supply voltage	V_{DD}	Note 1 Vss −0.5	7.0	V
Input voltage	V_I	Note 1 Vss −0.5	V_{DD} +0.5	V
Output voltage	V_O	Note 1 Vss −0.5	V_{DD} +0.5	V
Operational temperature	Topr	−20	75	°C
Storage temperature	Tstg	−55	150	°C

Note 1) Vss=0V

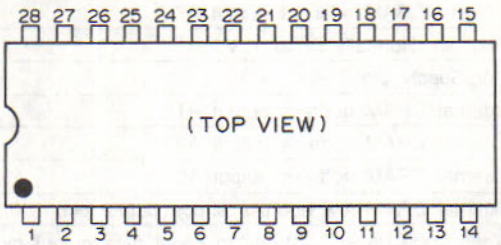
Block Diagram



Note) Pin numbers are those of CXD1160AP

Pin Configuration and Descripion (CXD1160AP)

Pin Configuration



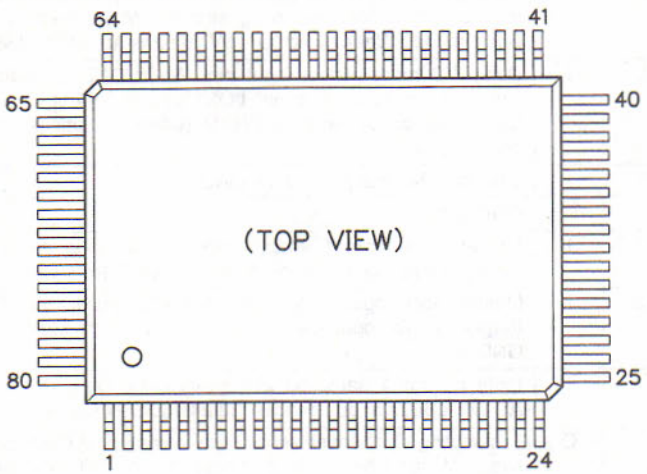
Pin Description

No.	Symbol	I/O	Description
1	SDT	I	Serial data input pin that receives commands, coefficient and I/O control transfer from the microcomputer. In each transfer modes, single 40-bit block is transferred at a time.
2	SCK	I	SDT serial clock input pin. Takes in data with the rising edge.
3	XSLD	I	Latch input pin that serves to latch inside the IC 1 block of serial data 40bit in length active at 'L'.
4	SIO2	I	Input pin. Sets the number of BCK clocks used for data transfer per channel (ch1 and 2) in one sampling section. When fixed to GND it turns to 32bit clock mode. When fixed to +5V it turns to 24bit clock mode.
5	DYSL	I	Delay I/O mode select input pin. When GND is fixed it turns to serial mode. Operates similarly as serial I/O. Fixed at +5V it turns to delay mode. Connected to an external DRAM (64kbit) composes a delay line for 2 channels.
6	TST	I	Test pin. Normally fixied to GND.
7	Vss	–	GND pin.
8	MCK1	I	Master clock input 1. Master clock ACK inside the IC is half this frequency. To input the master clock through MCK1 fix MCK 2 to +5V.
9	MCK2	I	Master clock input 2. Master clock ACK inside the IC has the same frequency. To input the master clock through MCK2 fix MCK1 to +5V or to GND.
10	SI	I	Input pin for 1 sampling 2ch serial data. Data format complement on two. At last LSB, various modes 32/24/16bit available.
11	SO	O	1 sampling 2 channel serial data output pin. Data format complement on two. At last LSB, various modes 32/24/16bit available.
12	BCK	I	Serial bit clock input pin of serial input data SI and serial output data SO. With the rising edge of this BCK serial input data is taken in and with the falling edge serial output data is sent out.
13	LRCK	I	Serial I/O sampling frequency clock input pin. Transfers ch1 data when level at 'H' and ch 2 data when level at 'L'.
14	XOVF	O	Adder-subtracter overflow detection output. Outputs 'L' during overflow detection.
15	A6	O	External DRAM address output A6
16	A3	O	External DRAM address output A3
17	A4	O	External DRAM address output A4
18	A5	O	External DRAM address output A5

No.	Symbol	I/O	Description
19	A7	O	External DRAM address output A7
20	XCLR	I	Test pin. Normally fix to +5V
21	V_{DD}	–	+5V Supply pin
22	A1	O	External DRAM address output A1
23	A2	O	External DRAM address output A2
24	A0	O	External DRAM address output A0
25	XRAS	O	External DRAM low address strobe output pin
26	XWSO	O	When DYSL is at 'L', turns to serial data output pin, and operates according to the various serial I/O modes. When DYSL is at 'H' turns into the write enable output pin of the external DRAM.
27	DIO	I/O	Turns to serial data input pin when DYSL is at 'L' and takes in according to the various serial I/O modes. Turns into external DRAM data I/O pin when DYSL is at 'H' to assume a common bus with DRAM data input D_{IN} and data output D_{OUT}.
28	XCAS	O	External DRAM column address strobe output pin

Pin Configuration and Pin Description (CXD1160AQ)

Pin Configuration



Pin Description

No.	Symbol	I/O	Description
1–3	N.C		
4	TST	I	Test pin. Normally fixed to GND.
5–8	N.C		
9	V_{SS}	–	GND pin
10–15	N.C		
16	MCK1	I	Master clock input 1. Master clock ACK inside the IC is half this frequency. To input the master clock through MCK 1 fix MCK2 to +5V.

No.	Symbol	I/O	Description
17–20	N.C		
21	MCK2	I	Master clock input 2. Master clock ACK inside the IC has the same frequency. To input the master clock through MCK2 fix MCK1 to +5V or to GND.
22–26	N.C		
27	SI	I	Input pin for 1 sampling 2ch serial data. Data format complement on two. At last LSB various modes 32/24/16 bit available.
28	SO	O	1 sampling 2 channel serial data output pin. Data format complement on two. At last LSB, various modes 32/24/16bit available.
29	BCK	I	Serial bit clock input pin of serial input data SI and serial output data SO. With the rising edge of this BCK serial input data is taken in and with the falling edge serial output data is sent out.
30	LRCK	I	Serial I/O sampling frequency clock input pin. Transfers ch1 data when level at 'H' and ch 2 data when level at 'L'.
31	XOVF	O	Adder-subtracter overflow detection output. Outputs 'L' during overflow detection.
32–33	N.C		
34	A6	O	External DRAM address output A6
35	A3	O	External DRAM address output A3
36	A4	O	External DRAM address output A4
37	A5	O	External DRAM address output A5
38	A7	O	External DRAM address output A7
39–43	N.C		
44	XCLR	I	Test pin. Normally fixed to 5V.
45–48	N.C		
49	V_{DD}	–	+5V supply pin
50–55	N.C		
56	A1	O	External DRAM address output A1
57–60	N.C		
61	A2	O	External DRAM address output A2
62–66	N.C		
67	A0	O	External DRAM address output A0
68	XRAS	O	External DRAM low address strobe output pin.
69	XWSO	O	When DYSL is at 'L', turns to serial data output pin, and operates according to the various serial I/O modes. When DYSL is at 'H' turns into the write enable output pin of the external DRAM.
70	DIO	I/O	Turns to serial data input pin when DYSL is at 'L' and takes in according to the various serial I/O modes. Turns into external DRAM data I/O pin when DYSL is at 'H' to assume a common bus with DRAM data input D_{IN} and data output D_{OUT}.
71	XCAS	O	External DRAM column addess strobe output pin.
72–73	N.C		

No	Symbol	I/O	Description
74	SDT	I	Serial data input pin that receives commands, coefficient and I/O control transfer from the microcomputer. In each transfer modes, single 40-bit block is transferred at a time.
75	SCK	I	SDT serial clock input pin. Takes in data with the rising edge.
76	XSLD	I	Latch input pin that serves to latch inside the IC 1 block of serial data 40bit in length active at 'L'.
77	SIO2	I	Input pin. Sets the number of BCK clocks used for data transfer per channel (ch1 and 2) in one sampling section. When fixed to GND it turns to 32bit clock mode. When fixed to +5V it turns to 24bit clock mode.
78	DYSL	I	Delay I/O mode select input pin. When GND is fixed it turns to serial mode. Operates similarly as serial I/O. Fixed at +5V it turns to delay mode. Connected to an external DRAM (64kbit) composes a delay line for 2 channels.
79–80	N.C		

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Operating temperature	Topr	−20		75	°C

Electrical Characteristics

DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Topr=−20 to 75°C)

Item		Symbol	Conditions	Min.	Max.	Unit
Output voltage (1)	H level (1)	V_{OH} (1)	I_{OH}=−2mA	V_{DD} −0.5V	V_{DD}	V
	L level (1)	V_{OL} (1)	I_{OL}= 4mA	V_{SS}	0.4	V
Note1 Input voltage (1)	H level (1)	V_{IH} (1)		2. 2		V
	L level (1)	V_{IL} (1)			0.8	V
Note 2 Input voltage (2)	H level (2)	V_{IH} (2)		0.7 V_{DD}		V
	L level (2)	V_{IL} (2)			0.3 V_{DD}	V
Input leak current		I_{LI}	V_I=0V to V_{DD}	−10	10	µA
Input leak current	Note3	I_{LZ}		−40	40	µA

Note 1) TTL input pin (CXD1160AP–27 pin, CXD1160AQ–70 pin)
Note 2) CMOS input pin
Note 3) During tristate pin input

Input/Output Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	CIN			12	pF
Output pin	COUT			12	pF
I/O pin	CI/O			12	pF

Test Conditions V_{DD}=V_I=0V, f=1MHz

Operation

Block Diagram Description

(1) I-RAM

I-RAM Instruction RAM with command word length of 24bit × 64 word. Write in from the exterior possible through microcomputer interface. Commands are divided into 1/2/3/ cycle commands according to type. Jumps to No. 0 every sampling cycle.

1-address stack 6bit address 2-stage stack. Combination with double sub routine or loop jump is possible.

Loop Counter 4bit loop counter. Loop jump possible from 0 to 15 times.

(2) K-RAM

K-RAM 16bit × 64 word coefficient RAM. Write in from the exterior can be performed through the microcomputer interface as well as write through execution command coefficient is in the format of complement on two while single precision (16b) and double precision (32b) are handled concurrently.

(3) D-RAM

D-RAM 16bit × 64 word data. Address space is ring shaped while the method adopted is for users to make access without knowledge of the physical address. Data is in the format of complement on two with single (16b) and double precision (32b) are handled concurrently.

D-address Counter 6bit long address counter counted up every sampling cycle. Users are aware of the address relative to that of the address counter value. The counter indicates the actual physical address and can be handled as a delay tap fixed address.

(4) Data Register (all in complement on two format)

SI1 Register This register (32b) stores CH1 data input from serial I/O used for read only. Upper 16bit (I1H) and lower 16bit (I1L) can be handled independently.

SI2 Register This register (32b) stores CH2 data input from serial I/O used for read only. Upper 16bit (I2H) and lower 16bit (I2L) can be handled independently.

SO1 Register This register (32b) stores CH1 data output from serial I/O. Beside read/write, can also be handled as a temporary register. upper 16bit (O1H), and lower 16bit (O1L) can be handled independently.

SO2 Register This register (32b) stores CH2 data output from serial I/O. Beside read/write, can also be handled as a temporary register. Upper 16bit (O2H) and lower 16bit (O2L) can be handled independently.

DI Register This register (32b) stores CH1 or CH2 data input from delay I/O. Used for read only. Upper 16bit (DIH) and lower 16bit (DIL) can be handled independently.

DO Register This register (32b) stores CH1 or CH2 data output from delay I/O. Used for write only. Upper 16bit (DOH) and lower 16bit (DOL) can be handled separately.

P Register This register 33bit in length, stores the multiplied results of various bit lengths.

R Register Data set in this register (32b) through the transfer command can be utilized as one sided input to AV. Upper 16bit (RH) and lower 16bit (RL) can be set independently.

ACC Register — This 34bit long register stores AU operation results. However during comparison commands ('ACC-R' or 'ACC-4R') values are not renewed.

(5) MPY

MOA Selector — Selects either K-RAM data or data from various registers called out through the bus, by means of the multiplying command.

MOB Selector — Selects either D-RAM data or data from various registers called out through the bus, by means of the multiplying command.

MPY — Data selected by means of the above 2 selectors is multiplied together. There are 4 ways of multiplying K*D, K*X, X*D and X*X. Also 4 multiplying modes 16b*16b, 16b*32b, 32b*16b and 32b*32b.

(6) AU

AOA Selector — Selects either ACC or O by means of AU command

AOB Selector — Selects either P (33b) or R (32b) to convert into 34 bit length

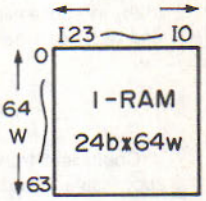
AU — Data selected by means of the above 2 selectors is either added, subtracted, turned into absolute value or compared together.

Clipper — When ACC data is transferred or multiplied, or sent to the below mentioned barrel shifter via the bus, clip processing is executed on the 34bit length to obtain a 32bit length. During transfer or multiplying the upper 16bit of this output (ACCH) and the lower 16bit (ACCL) can be handled independently

Barrel Shifter — ACC value passed through the clipper can be handled as follows 1) converted into positive value floating point form 2) arithmetic left shift executed 3) arithmatic right shift executed.

Internal RAM structure

I-RAM



Instruction RAM (I-RAM) integrated in CXD1160AP/AQ is composed of address 0 to 63 (24b*64w) with a command word length of 24bit. Commands are transferred one (24bit) at a time through the microcomputer interface mode 1, from the exterior. Each transfer can be sent to the desired address.

External interrupt is executed at serial I/O LRCK and BCK. Every sampling cycle a jump is forcibly made to 0 address. That is, at every sampling the command is repeatedly executed from 0 address.

For executive commands there are, forced jump (JMP), condition jump, sub routine call (CAL), sub routine turn (RTN) and loop jump (LPJ). They all fly to the absolute address.

There are 2 stack stages and usage in conjunction with double sub routine or loop jump is possible.

Loop counter is conposed of 4bit and loop jump can be executed up to 15 times.

Command execution cycle is given according to MPY mode in 1/2/3/ cycle time.

The number of cycles that can be executed within 1 sampling section depends on the sampling frequency (fs) and the cycle clock ($f_{KCK}=f_{ICK}$). Let's assume that at sampling section 1 we have L cycle (cycle 0 to cycle L-1). Here, the last cycle (L-1) called KSH cycle cannot be executed because of the command or coefficient transfer section of the microcomputer interface. Cycle (L-2) called KSL cycle can be executed with the exception of K-RAM handling.

Example 1) $f_S=48kHz$ $f_{KCK}=\frac{1}{4}f_{MCK1}=\frac{1}{2}f_{MCK2}=6.144MHz(=48k\times128)$

In this case $f_{KCK}/f_S=128$. There are 128 cycles (cycle 0 to 127).

Cycle 0 to cycle 125 ..... Execution cycle
Cycle 126 ..... Execution possible with the exception of K-RAM handling.
Cycle 127 ..... Execution impossible

Example 2) $f_S=44.1k$ $f_{KCK}=6.144M$

In this case at $f_{KCK}/f_S=139.3...$ both 139 cycle (cycle 0 to cycle 138) and 140 cycle (cycle 0 to cycle 139) exist.

Cycle 0 to cycle 136 ..... Execution cycle
Cycle 137 ..... Execution possible with the exception of K-RAM handling
Cycle 138, 139 ..... Execution impossible.

The sequencial execution address of 63 address is 0 address.
When Power is ON the contents of I-RAM are not determined.

K-RAM

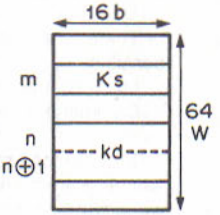
Coefficient RAM (K-RAM) built-in CXD1160AP/AQ is composed of 16bit × 64 word (address 0 to address 63). Single precision coefficient 1w (16b), double precision coefficient are expressed by 2w (32b) in succession, and can coexist on K-RAM. In the operation system both are complement on 2 and MSB can be handled as $1 > K \geq -1$ at Sign bit.

$$Ks = -K_{15} + \sum_{i=1}^{15} 2^{-i} K_{15-i} \qquad Kd = -K_{31} + \sum_{i=1}^{31} 2^{-i} K_{31-i}$$

Coefficient transfers from the exterior in the microcomputer interface K mode the required successive 2 addresses (32b) at one time. As there is also inside the execution command a command that serves to write in K-RAM, one part can be used as a temporary register. At Power ON K-RAM contents are undetermined.

Referring to the fig on the right the storage position can be defined as follows.

- When m address single precision is specified, the single precision coefficient Ks in m address can be used.
- When n address double precision is specified, the double precision coefficient kd in n address n⊕ address 1 can be used. Here low word K_L is stored in n address and high word K_H is stored in n⊕ 1 address.



K-RAM address specify can be mentioned in the command that actually handles K-RAM. There are 2 types of K-RAM address specify absolute address specify and relative address specify.

- Absolute adderss specify Absolute address→addr
- Relative address specify addr⊕relative address→addr

During commands that do not handle K-RAM, the present address addr does not change. (addr→addr)

At the forced 0 address jump every sampling cycle, reset is executed to addr=0. Accordingly and for the first time only, both the absolute address specify and relative address specify indicate the same physical address.

When double precision command is utilized with addr, after the command execution, addr+1→addr is obtained. Note that the present address obtained is 1 increment over that of the address specified from the user side.

Address 63 and address 0 are ring addresses. (0⊕−1=63, 63⊕1=0)

As a total of 2 cycles, the last cycle of the sampling section and the cycle before that, are coefficient transfer sections, K-RAM cannot be utilized.

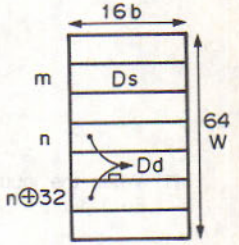
D-RAM

Data RAM(D-RAM) built-in CXD1160AP/AQ is organized in 16 bit × 64 word (address 0 to address 63). Single precision data is indicated in 1W (16b) and double precision data at a 32 address distance in 2W (32b). Both can be disposed on D-RAM. For operations both are used with complement on two. MSB is at Sign Bit to be handled as $1 > D \geqq -1$. D-RAM contents is unspecified at Power On.

$$Ds = -D_{15} + \sum_{i=1}^{15} 2^{-i} D_{15-i} \qquad Dd = -D_{31} + \sum_{i=1}^{31} 2^{-i} D_{31-i}$$

Referring to the fig. on the right the storage position can be defined as follows.

- When m address single precision is specified, single precision data Ds can be used.
- When n address double precision is specified, double precision data Dd in n ⊕ address 32 can be used. Here high word D_H is stored in n address and low word D_L in n ⊕ address 32.



D-RAM address specification by users is a logical address and not a physical one.
Inside the IC there is a 6 bit ring address counter that is incremented every I/O sampling. The logical address addr which is modulo added to this counter value DAC because the physical address.

Physical address=DAC ⊕ addr

Example) Logical address is assigned to the respective data in the formula at right.

formula: $y(n)=k_1y(n-1)+k_2X(n)+k_3X(n-1)$

addr: 3 2 1 0

If y(n) is entered in addr=3 and X(n) in addr=1 then y(n-1) is constantly in addr=2 and X(n-1) in addr=0

Physical address⇨	4	3	2	1	0
DAC=0 n		y(n)	y(n-1)	X(n)	X(n-1)
DAC=1 n+1 →n	y(n)	y(n-1)	X(n)	X(n-1)	X(n-2)

D-RAM address specify can be mentioned in the command that actually handles D-RAM.
There are 2 types of address specify, absolute address specify and relative address specify.

- Absolute address specify — Absolute address → addr
- Relative address specify — addr ⊕ relative address → addr

With commands where there is no D-RAM address specify, the present address addr remains unchanged. (addr → addr).
Reset to addr=0 is effected at address 10 forable jump every sampling cycle. Accordingly and for the first time only, absolute address specify and relative address specify indicate the same logical address.
Address 63 and address 0 are ring addresses (0⊖1=63, 63⊕1=0)

Note that double precision data low word side is far away to determine all the data location.

The last cycle in the sampling section is a command transfer section and commands cannot be executed.

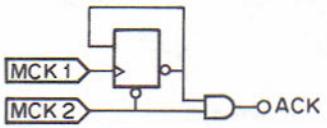
Interface

Clock circuit

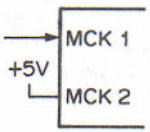
There are 2 methods to generate the master clock ACK in this IC.

(1) The clock input from MCK1 input pin is frequency divided by 2 internally to be ready for use.

(2) The clock input from MCK2 input pin is directly used.

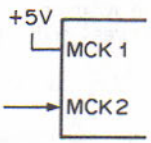


(1) When the input is from input pin MCK1
Fix input pin MCK2 to +5V



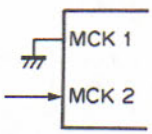
$$f_{MCK1} = 2f_{ACK}$$

(2) When the input is from input pin MCK2
Fix input pin MCK1 to +5V or to GND



$$f_{MCK2} = f_{ACK}$$

In any case the maximum frequency of master clock ACK is



$$f_{ACK} \leqq 15.36\text{MHz}(=48\text{K} \times 320)$$

Moreover as this IC makes use of a dynamic F/F internally, it is not possible to stop the the master clock and keep the internal condition as it is.

Cycle clock ICK (or KCK) inside the IC is twice ACK master clock.

$$f_{ICK} = f_{KCK} = \frac{1}{2} f_{ACK}$$

Commands differ according to type. There are 1 cycle/2 cycle and 3 cycle commands.

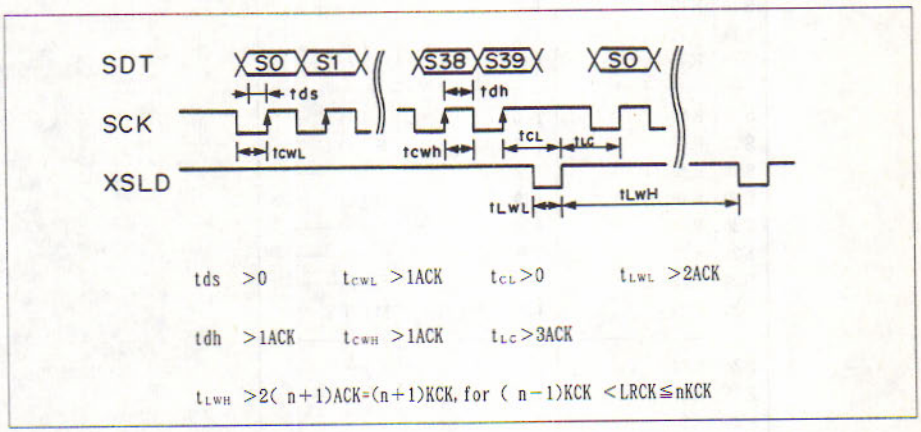
Microcomputer interface

There are 3 input pins used for microcomputer control. Those are used to rewrite in part or totally K-RAM or I-RAM inside the IC, as well as to execute the various settings of serial I/O and delay I/O.

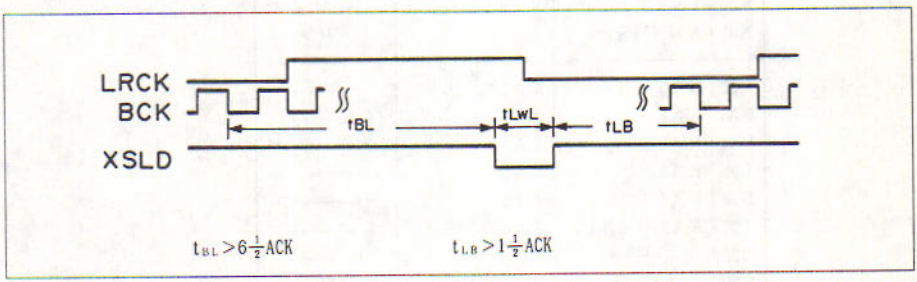
• SDT	40 bit in length of serial data per transfer.
• SCK	This serial clock transfers serial data to the internal shift register at the rising edge.
• XSLD	This gate pulse (active low level) latches in a lump the 40 bit serial data input to the shift register. At the same time and with this rising edge processing inside the IC is requested.

* When this IC is used as a multi-processor, all SDT pins or SCK pins on the respective IC's may be linked.

The transfer format (shown later on) timing system features serial data from S0 (top bit) to S39 as shown in the big below.



By applying the below conditions to XSLD the above t_{LWH} conditions can be prevented and the max. Transfer rate of 40 bit/LRCK realized.



The setting contents transferred through this microcomputer interface are undetermined inside the IC when Power is ON.
SDT, SCK and XSLD timing is regulated inside the IC before usage.

Transfer format

	K mode	I mode	R mode
S0	K0 (LSB)	I0	R0 (LSB)
S1	K1	I1	R1
S2	K2	I2	R2
S3	K3	I3	R3
S4	K4	I4	R4
S5	K5	I5	R5
S6	K6	I6	R6
S7	K7	I7	R7
S8	K8	I8	R8
S9	K9	I9	R9 (MSB)
S10	K10	I10	———
S11	K11	I11	———
S12	K12	I12	———
S13	K13	I13	———
S14	K14	I14	———
S15	K15	I15	———
S16	K16	I16	SIO0
S17	K17	I17	SIO1
S18	K18	I18	———
S19	K19	I19	DIO
S20	K20	I20	———
S21	K21	I21	———
S22	K22	I22	———
S23	K23	I23	MUTE
S24	K24	———	———
S25	K25	———	———
S26	K26	———	———
S27	K27	———	———
S28	K28	———	———
S29	K29	———	———
S30	K30	———	———
S31	K31 (MSB)	<L>	<H>
S32	KA0 (LSB)	IA0 (LSB)	———
S33	KA1	IA1	———
S34	KA2	IA2	———
S35	KA3	IA3	———
S36	KA4	IA4	———
S37	KA5 (MSB)	IA5 (MSB)	———
S38	———	———	———
S39	<L>	<H>	<H>

* In brackets < > respective modes proper value
* Between "——"=don't care

(1) K mode

This mode transfers the coefficient (complement on 2 and MSB at sign bit) to K-RAM (16bit × 64w). S39 is at 'L'.

With the 6 bits of KA5 (MSB) to KA0 K-RAM address (address 0 to 63) is specified. 16 bits, K15 to K0 are input from MSB side to KA address. 16 bits, K31 to K16 are input from MSB side to KA⊕1 address. When KA specifies address 63, KA⊕1 goes to 0 address.

When K31 to K0 are at double precision coefficient (32bits), handle through the low word side KA address for instructions.

$$K_{KA} = -K_{31} + \sum_{i=1}^{15} 2^{-i} K_{31-i}$$

Then,

If K15 to K0 or K 31 to K 16 are at single precision coefficient(16bit)

$$K_{KA} = -K_{15} + \sum_{i=1}^{15} 2^{-i} K_{15-i} \quad \text{or} \quad K_{KA+1} = -K_{31} \oplus \sum_{i=1}^{15} 2^{-i} K_{31-i}$$

Then,

Whatever the contents be, there is no change as far as the transfer of a 2 word part to an address where KA and KA⊕1 are in succession, is executed each time.

Moreover,note that there are write in commands to K-RAM in the instructions too.

(2) I mode

This mode transfers instructions to I-RAM (24 bit × 64W) S39 is at 'H' and S 31 at 'L'. IA5 (MSB) to IA0 (LSB) 6 bit specify I-RAM address IA (address 0 to 63). To this IA address I23 to I0 24 bit are input.

(3) R mode

This mode transfers information relative to the setting of serial I/O and Delay I/O.

S39 is at 'H' and S31 at 'H' too.

Beside this, setting is executed at pins DYSL and SIO2 of the IC according to requirements.

DYSL	Delay I/O
Fix to GND	Serial mode
Fix to +5V	Delay mode

SIO2	Bit clock (BCK)
Fix to GND	32 bit clock mode
Fix to +5V	24 bit clock mode

□ $\overline{\text{MUTE}}$

Controls serial I/O output (SO) and output (XWSO) during delay I/O serial mode.

When delay I/O is in delay mode, only serial I/O is controlled.

The actual MUTE switching is synchronous with the rising edge of LRCK and serial output data. In any case, serial output data doesn't change in the middle of a bit.

$\overline{\text{MUTE}}$	Serial I/O output	Delay I/O (Serial mode) output
"L" Mute ON	0 (all L)	0 (all L)
"H" Mute OFF	Serial out register value	Delay out register value

☐ DIO
Sets the bit length of delay sample data during Delay I/O delay mode.

DIO	Delay data	Conditions to be met for proper operation
"L"	30 bit length	LRCK≧128KCK=256ACK
"H"	32 bit length	LRCK≧136KCK=272ACK

☐ SIO1, SIO0
In combination with IC Pin SIO2, select I/O format of serial I/O and Delay I/O (Serial mode)

SIO2	SIO1	SIO0	Bit clock	IN data		Out data
GND	X	X	32 clock	32 bit	——	32 bit
+5V	L	L	24 clock	16 bit	——	24 bit
"	L	H	"	24 bit	——	24 bit
"	H	L	"	24 bit	——	16 bit
"	H	H	"	16 bit	——	16 bit

☐ R9 to R0
Sets the delay sample quantity common to Delay I/O (delay mode) 2ch number of delay samples.

R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Number of delay samples
L	L	L	L	L	L	L	L	L	L	1
H	H	H	H	H	H	H	H	H	H	2
H	H	H	H	H	H	H	H	H	H	3
H	H	H	H	H	H	H	H	H	H	4
				⟆						⟆
L	L	L	L	L	L	L	L	H	H	1022
L	L	L	L	L	L	L	L	H	L	1023
L	L	L	L	L	L	L	L	L	H	1024

Control bits not in usage may be set to either H or L.
For Serial I/O and Delay I/O see different paragraph for details.

Serial I/O

Serial data interface I/O corresponding to 16 bit stereo D/A converter (CX20152) format.
One each for input and output, operate in common synchronously with external LRCK and BCK.
Each inputs and outputs data for 2ch at every sample cycle. For bit clock BCK there are 2 kinds, 32 bit clock mode and 24 bit clock mode.
Data format is in complement on 2 positive logic binary fixed decimal point type.
There is 32 bit/24 bit/16 bit data according to the various modes. Transfer order for each and all is at the last LSB.

Pin	I/O	Contents
LRCK	IN	Serial mode clock (Sampling cycle clock). Transfers channel 1 at H level and channel 2 at L level.
BCK	IN	Serial data bit clock. Features for each channel 32 bit clock mode and 24 bit clock mode.
SI	IN	Serial data input. Takes in synchronously with BCK rising edge.
SO	OUT	Serial data output. Outputs synchronously with BCK falling edge.

Inside the IC the following registers are compatible with Serial I/O. Handling is possible in 16 bit or 32 bit units.

Reg.	Contents	bit length	R/W	Bit expression for later mention
I1H	Channel 1 input high word register	16	R	A_{31} A_{30} ---------- A_{17} A_{16}
I1L	Channel 1 input low word register	16	R	A_{15} A_{14} ---------- A_{1} A_{0}
I2H	Channel 2 input high word register	16	R	B_{31} B_{30} ---------- B_{17} B_{16}
I2L	Channel 2 input low word register	16	R	B_{15} B_{14} ---------- B_{1} B_{0}
O1H	Channel 1 output high word register	16	R/W	C_{31} C_{30} ---------- C_{17} C_{16}
O1L	Channel 1 output low word register	16	R/W	C_{15} C_{14} ---------- C_{1} C_{0}
O2H	Channel 2 output high word register	16	R/W	D_{31} D_{30} ---------- D_{17} D_{16}
O2L	Channel 2 output low word register	16	R/W	D_{15} D_{14} ---------- D_{1} D_{0}

For Instructions read only available for input register. For output register either read or write available. For use as single precision (16 bit) register, the above 8 registers can all be handled independently. For instance when I1H is specified the numerical expression becomes, A_{31} at MSB (sign bit) and A_{16} at LSB

$$A_s = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i}$$

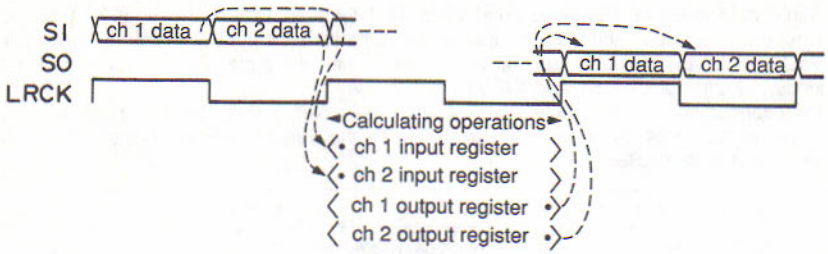
For use as double precision (32 bit) register, I1H/L, I2H/L, O1H/L and O2H/L come in pairs. For instance when I1H is specified the numerical expression becomes, A31 at MSB (sign bit) and A0 at LSB.

$$A_d = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i}$$

This is not usual but when I1L is specified at double precision, numerical expression becomes A15 at MSB (sign bit) and A16 at LSB.

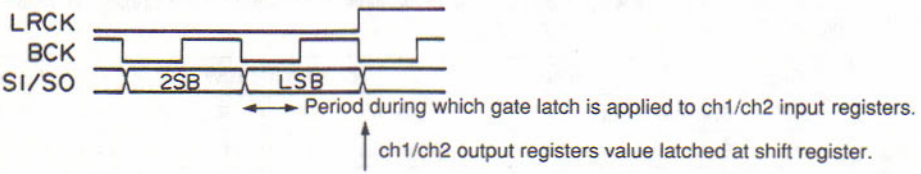
$$A_d = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i} + \sum_{i=1}^{15} 2^{-16-i} A_{31-i}$$

Outline of Serial I/O timing



First, during 1LRCK period, ch1/ch2 serial data that is input from SI is latched at ch1/ch2 input register with the rising edge of the following LRCK. Also,during 1LRCK, if the results of the calculating operations are enclosed into ch1/ch2 output registers, those are latched by the shift register at the following rising edge of LRCK to be respectively output as serial data from SO.

Detailed timing between Serial I/O and I/O register is as follows.



Serial I/O and I/O register are dependent on the timing with LRCK and BCK from the exterior. Also the only interrupt is executed between this LRCK and BCK on the Instructions.

The IC operates on the master clock. Now, should the operation be going on in 1LRCK period at cycle 0 to cycle L (L+1 cycle), the following restrictions would apply to the I/O register handling.

<Input register read command>

Cycle (L-3), (L-2), (L-1), L cannot read.

Cycle 0 to cycle (L-4) can read.

<Output register write command>

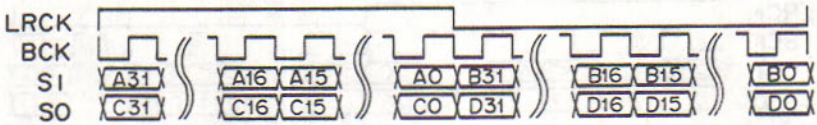
The following are standards of cycles where write cannot be executed in the output register. This is because of the frequency relationship between bit clock BCK and cycle clock KCK (ICK).

Order of cycle	24 clock mode	32 clock mode
L-3	12KCK ≧LRCK≧ 0	16KCK ≧LRCK≧ 0
L-2	60KCK 〃 0	80KCK 〃 0
L-1	108KCK 〃 0	144KCK 〃 0
L	all	all
0	LRCK ≧ 132KCK	LRCK≧176KCK
1	LRCK ≧ 180	LRCK ≧ 240
2	LRCK ≧ 228	LRCK ≧ 304
⋮		
n	LRCK ≧ 132+48n	LRCK ≧ 176+64n

(1) 32 bit clock mode 32 bit IN-32 bit OUT

SIO2	SIO1	SIO0
GND	×	×

Timing



Register

	MSB	(LSB)	(MSB)	LSB
I1H	A_{31} A_{30} ····· A_{17} A_{16}	I1L	A_{15} A_{14} ····· A_1 A_0	
I2H	B_{31} B_{30} ····· B_{17} B_{16}	I2L	B_{15} B_{14} ····· B_1 B_0	

	MSB	(LSB)	(MSB)	LSB
O1H	C_{31} C_{30} ····· C_{17} C_{16}	O1L	C_{15} C_{14} ····· C_1 C_0	
O2H	D_{31} D_{30} ····· D_{17} D_{16}	O2L	D_{15} D_{14} ····· D_1 D_0	

If all data is handled as 32 bit data then, we have 2ch IN 2ch OUT.
If all data is handled as 16 bit data, then we have 4ch IN 4ch OUT.
Mixed handling in single precision (16 bit) and double precision is possible.

Example of Single precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i} \qquad I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i}$$

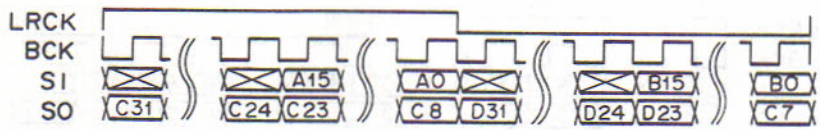
Example of Double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i}$$

(2) 24 bit clock mode 16 bit IN-24 bit OUT

SIO2	SIO1	SIO0
+5V	L	L

Timing



Register

		MSB	LSB
I1H	×·····×	I1L	A_{15} A_{14} ·····A_1 A_0
I2H	×·····×	I2L	B_{15} B_{14} ·····B_1 B_0

	MSB		LSB 8LSB
O1H	C_{31} C_{30} ·····C_{17} C_{16}	O1L	C_{15} C_{14} ·····C_8× ·····×
O2H	D_{31} D_{30} ·····D_{17} D_{16}	O2L	D_{15} D_{14} ·····D_8× ·····×

Input register enters on low word register side. Output register is at lower 8 bit don't care.

Example of single precision numerical expression

$$I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i}$$

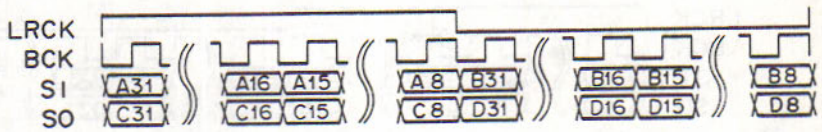
Example of double precision numerical expression

$$O1H = -C_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} \Rightarrow -C_{31} + \sum_{i=1}^{23} 2^{-i} C_{31-i}$$

(3) 24 bit clock mode 24 bit IN-24 bit OUT

SIO2	SIO1	SIO0
+5V	L	H

Timing



Register

	MSB		LSB	8LSB
I1H	A_{31} A_{30} ····· A_{17} A_{16}	I1L	A_{15} A_{14} ····· A_8 0 ····· 0	
I2H	B_{31} B_{30} ····· B_{17} B_{16}	I2L	B_{15} B_{14} ····· B_8 0 ····· 0	

	MSB		LSB
O1H	C_{31} C_{30} ····· C_{17} C_{16}	O1L	C_{15} C_{14} ····· C_8 × ····· ×
O2H	D_{31} D_{30} ····· D_{17} D_{16}	O2L	D_{15} D_{14} ····· D_8 × ····· ×

0 is input in the lower 8 bit of the input register, while the output register lower 8 bit are at don't care.
24 bit 2ch IN-24 bit 2ch OUT.
Can be handled as the data between 16 bit and 8 bit.

Example of single precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i} \qquad I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i} = -A_{15} + \sum_{i=1}^{7} 2^{-i} A_{15-i}$$

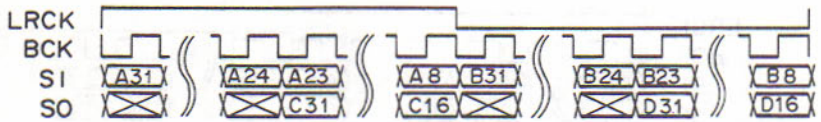
Example of double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} \Rightarrow -A_{31} + \sum_{i=1}^{23} 2^{-i} A_{31-i}$$

(4) 24 bit clock mode 24 bit IN-16 bit OUT

SIO2	SIO1	SIO0
+5V	H	L

Timing



Register

	MSB			LSB	8 LSB
I1H	A_{31} A_{30} ····· A_{17} A_{16}	I1L	A_{15} A_{14} ····· A_8	0	····· 0
I2H	B_{31} B_{30} ····· B_{17} B_{16}	I2L	B_{15} B_{14} ····· B_8	0	····· 0

	MSB	LSB		
O1H	C_{31} C_{30} ····· C_{17} C_{16}	O1L	×	····· ×
O2H	D_{31} D_{30} ····· D_{17} D_{16}	O2L	×	····· ×

In the input register lower 8 bit there are eight 0's. The output register uses the high word side. Accordingly O1L and O2L are used as temporary registers.

Example of single precision numerical expression

$$O1H = -C_{31} + \sum_{i=1}^{15} 2^{-i} C_{31-i}$$

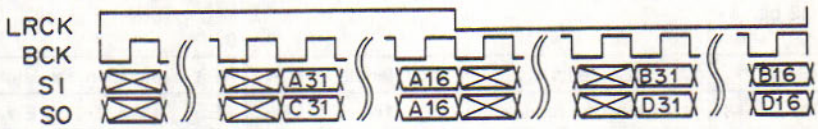
Example of double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} = -A_{31} + \sum_{i=1}^{23} 2^{-i} A_{31-i}$$

(5) 24 bit clock mode 16 bit IN-16 bit OUT

SIO2	SIO1	SIO0
+5V	H	H

Timing



Register

	MSB		LSB		
I1H	A_{31} A_{30} ·····	A_{17} A_{16}	I1L	×	×
I2H	B_{31} B_{30} ·····	B_{17} B_{16}	I2L	×	×

	MSB		LSB		
O1H	C_{31} C_{30} ·····	C_{17} C_{16}	O1L	×	×
O2H	D_{31} D_{30} ·····	D_{17} D_{16}	O2L	×	×

As the input register uses high word register only.
Accordingly I1L and I2L are not use. O1L and O2L are used as temporary registers.

Example of single precision numerical expression.

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i}$$

Delay I/O

There are 2 modes. When input pin DYSL is grounded serial mode is on. When it is set to +5V delay mode is ON.

Here serial mode means delay I/O operates similarly as serial I/O. Also, in delay mode DRAM is connected to the exterior and sample delay executed at will.

The following registers correspond to delay I/O inside the IC. Handling is either in units of 16 bit or 32 bit.

Reg.	Contents	bit length	R/W	Bit expression for later mention
DIH	Input high word register	16	R	E_{31} E_{30} ..... E_{17} E_{16}
DIL	Input low word register	16	R	E_{15} E_{14} ..... E_{1} E_{0}
DOH	Output high word register	16	W	F_{31} F_{30} ..... F_{17} F_{16}
DOL	Output low word register	16	W	F_{15} F_{14} ..... F_{1} F_{0}

In the Instructions, input register is for read only while output register is for write only.

When used as single precision register (16 bit), the 4 registers shown above may be used individually. That is when DIH is specified, numerical expression turns out as MSB at E_{31} and LSB at E_{16}.

for $$E_5 = -E_{31} + \sum_{i=1}^{15} 2^{-i} E_{31-i}$$

When used as double precision register (32 bit), DIH/L and DOH/L come in pairs. That is when DIH is specified, numerical expression turns out as MSB at E_{31} and LSB at E0.

for $$E_d = -E_{31} + \sum_{i=1}^{31} 2^{-i} E_{31-i}$$

as much as similarity with serial I/O register is concerned. However there is a decisive difference where the following points are concerned.

In serial I/O register two 32 bit stereo for 1ch each, are available. The 2 input registers maintain the same value for about 1LRCK. That is from the time both are input near LRCK rising edge until around the next LRCK rising edge. During this period read is possible any time. Move over after both the 2 output registers are output to S/R around LRCK rising edge, until the following LRCK rising edge and for about the period of 1LRCK, the next value to be output should be input. During this period, usage as temporary register is possible.

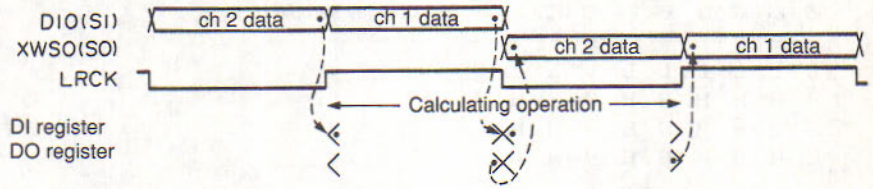
On the other hand, delay I/O register has only 32 bit 1ch. to stereo operate that, the input register has to be input twice during 1LRCK period.
Similarly the output register is output twice. Accordingly programs have to be written along those lines.

Delay I/O serial mode

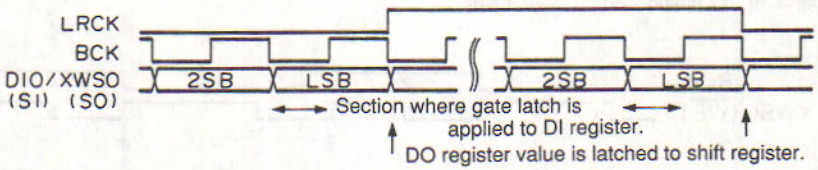
By fixing input pin DYSL to GND delay I/O turns to serial mode.

In this case delay I/O operates as serial I/O. That is the timing system is regulated by LRCK and BCK and the format by SIO2, SIO1 and SIO0. Also, serial input data is input and output from DIO/SI pin, and serial output data, from XWSO pin.

Delay I/O register is monoral. When it is input/output twice to 1LRCK, stereo operation is executed. An outline of delay I/O input/output system timing is as follows.



The detailed timing of delay I/O input/output register is as follows.



DI register value contained in the first half of 1LRCK calculating operations is the serial input data of the second half of the preceding LRCK. DI register value is similarly the serial input data of LRCK first half.

Also, the value entered to DO register in the first half becomes the serial output data of the same LRCK latter half in the 1LRCK calculating operations. The value entered in DO register during the second half becomes the serial output data in the first half of the following LRCK.

DI register read prohibit cycle around LRCK falling edge and DO register write prohibit cycle change in relation to LRCK, BCK and the original oscillation. DI or DO registers handling around this area should be performed after due confirmation.

During delay I/O serial mode, turn open the external DRAM pins for delay mode, that is XRAS, XCAS and A7 to A0, 10 in all.

Delay I/O delay mode

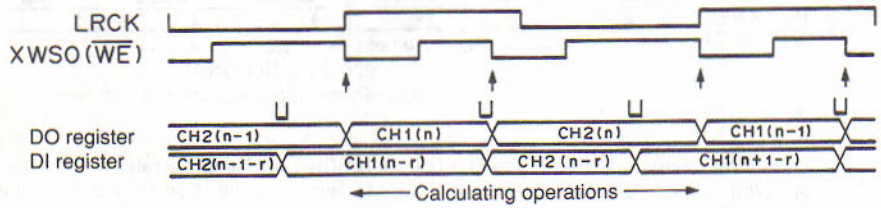
By fixing input pin DYSL to +5V, delay I/O turns to delay mode.
In this case, delay I/O composes the delay space by utilizing the 64K bit × 1 DRAM connected to the exterior.

64K × 1=1024 sample × (32 bit + 32 bit)

That is, 32 bit data 1 to 1024 sample stereo delay is performed. This stereo delay sample volume is set through the microcomputer interface R mode (R9 to R0).

R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	No. of delay sample r
L	L	L	L	L	L	L	L	L	L	1
H	H	H	H	H	H	H	H	H	H	2
H	H	H	H	H	H	H	H	H	L	3
H	H	H	H	H	H	H	H	L	H	4
				⌇						⌇
L	L	L	L	L	L	L	L	H	H	1022
L	L	L	L	L	L	L	L	H	L	1023
L	L	L	L	L	L	L	L	L	H	1024

Outline of the timing system is as follows.



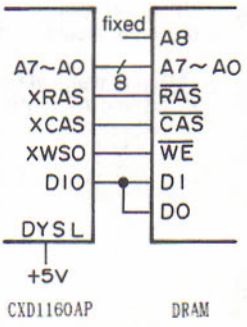
*DO register indicates data entered in the last part of that space.

That is if data CH1 (n) is written in DO register of 1LRCK (calculating operations) first half, then data CH1 (n-r) can be read from DI register. If data CH2 (n) is written in DO register at the second half, then data CH2 (n-r) can be read from DI register.

Connection to the external DRAM is as seen on the fig at right fixed.
Fix addresses over A8 to +5V or GND.

Moreover, for addresses that move frequently the order is: Column A0 to A4, Row A0 to A7, and column A5 to A7.

There are 2 kinds of data bit length for delay 32 bit and 30 bit. Timing system differs according to type.



(1) 32bit delay mode

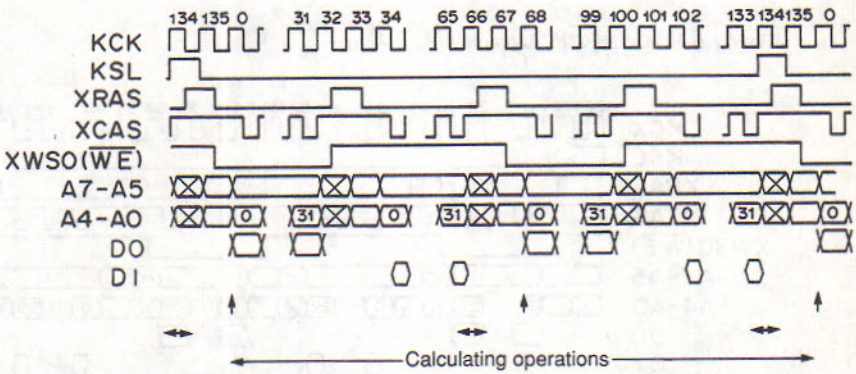
By turning DIO, of the microcomputer interface R mode to 'H', 32bit delay mode is set on. To realize this, the following hardware conditions should be met.

LRCK≧136KCK=272ACK

With 32bit delay mode, delay for all 32bit DI/DO registers is possible.

DIH	E_{31} E_{30} ····· E_{17} E_{16}	DIL	E_{15} E_{14} ····· E_1 E_0
DOH	F_{31} F_{30} ····· F_{17} F_{16}	DOL	F_{15} F_{14} ····· F_1 F_0

Timing (LRCK=136KCK Example)



Should the data written last between cycle 0 to 66 in DO register be at CH1(n), data CH1(n-r) from the previous cycle 134 up to the present cycle 65 in DI register can perform read.

Similarly, should data written last between cycle 68 and last cycle 1 in DO register be at CH2(n), data CH2(n-r) between cycle 66 to 133 in DI register can perform read.

(2) 30bit delay mode

By turning DIO, of the microcomputer interface R mode to 'L', 30bit delay mode is set on. To realize this, the following hardware conditions should be met.

$$LRCK \geqq 128KCK = 256ACK$$

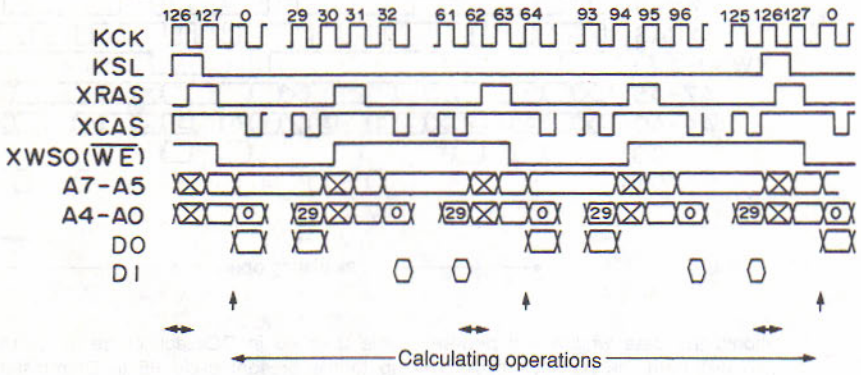
That is, 512 $f_{SMP} \leqq f_{MCK1}$ or 256 $f_{SMP} \leqq f_{MCK2}$

30bit delay mode can perform the delay of DI/DO register upper 30bit.

DIH	E_{31} E_{30} ····· E_{17} E_{16}	DIL	E_{15} E_{14} ····· E_3 E_2 0 0
DOH	F_{31} F_{30} ····· F_{17} F_{16}	DOL	F_{15} F_{14} ····· F_3 F_2 × ×

Here, DOL register lower 2bit are at don't care, DIL register lower 2bit contain 0.

Timing (LRCK=128KCK Example)



Should the data written last between cycle 0 to 62 in DO register be at CH1(n), data CH1(n-r) from the previous cycle 126 up to the present cycle 61 in DI register can perform read.

Similarly, should data written last between cycle 64 and last cycle 1 in DO register be at CH(n), data CH2(n-r) between cycle 62 to 125 in DI register can perform read.

Instructions

Outline

In one 24bit word length command the following can be executed in parallel. ① K-RAM and D-RAM address setting, ② MPY Command, ③ AU Command ④ Transfer Command ⑤ Jump Command. Data handled include, single precision (16b), double precision (32b) or through a combination of the 2, from 1 cycle to 3 cycle commands are available.

①K-RAM and D-RAM address setting

Sets the RAM address to be handled by a given command. For address setting there are, absolute address specify and relative address specify.

- K-RAM Single precision coefficient and double precision coefficient (2W in succession) can be used in this order or otherwise. Write is also enabled through a command allowing for use as a temporary register

- D-RAM Ring address. The modulo added value of the address counter value incremented at each serial I/O sampling cycle and that of the address set by the user becomes the actual value. Single precision data and double precision data (2W mutually separated by 32 addresses.) can be used in this order or otherwise.

②MPY Command

4 Types (K*D, K*X, X*D, X*X) and 4 kinds of modes (16b*16b, 16b*32b, 32b*16b, 32b*32b) can be handled. Through the respective modes the execution cycle of the command is determined.

K....K-RAM value D....D-RAM value

X....From the register related ones hanging to the main bus, those that can output Acc.

③AU Command

Can perform addition, subtraction, absolute value and comparison. A 2bit shifter is also biult-in.

④Transfer Command

Single precision data internally transfers double precision data via the main bus. Barrel shifter operations are executed through this transfer command.

⑤Jump Command

There are unconditional jump, conditional jump, subroutine call and return, loop jump. Stack features a 2-stage structure and combination with double sub routine or loop jump is possible. Loop counter can perform loop jump 0 to 15 times at 4b. At every serial I/O sampling cycle forced 0 address jump is executed.

Points in Execution Commands

Each execution command with a 24 bit word length can, widely speaking, process the following in parallel. RAM address setting, MPY command AU command, transfer command and jump command. Specially through MPY command, data to be handled is defined as single precision or double precision. According to what the execution cycle is determined.

Data register and data format

The following data resgisters relate to command execution

Symbol	bit	R/W	functions
I1H	16	R	Serial I/O channel 1 input high word register and low word register
I1L	16	R	
I2H	16	R	Serial I/O channel 2 input high word register and low word register
I2L	16	R	
O1H	16	R/W	Serial I/O channel 1 output high word register and low word register
O1L	16	R/W	
O2H	16	R/W	Serial I/O channel 2 output high word register and low word register
O2L	16	R/W	
D1H	16	R	Delay I/O input high word register and low word register
D1L	16	R	
DOH	16	W	Delay I/O output high word register and low word register
DOL	16	W	
RH	16	W	High word register and low word register for AU operations
RL	16	W	
P	33	—	Register where multiplication results are entered
Acc	34	—	Register where AU operation results are entered
AH AL	16 16	R R	High word and low word from the 32 bit that passed Clipper in Acc register value
BSI BSO	31 16	— R	Barrel shufter input register and output register

From the above commands that can execute Read become the source of transfer of the transfer command through the main bus or the multiplicator input data of MPY command.
In single precision (16b) commands, respective registers are handled independently. In double precision commands (32b) high word registers and low word registers are handled in pairs.

At power ON the respective registers data value become indefinite.

RAM address setting

(1) K-RAM address setting

Absolute address specify • K_6 (d) → addr

I12	I11 I10 I9 I8 I7 I6
H	a5 a4 a3 a2 a1 a0

At absolute expression 0 to 63

Relative address specify • addr ⊕ K_6 (r) → addr

I12	I11 I10 I9 I8 I7 I6
L	a5 a4 a3 a2 a1 a0

At complement on 2 expression −32 to +31

• addr ⊕ K_4 → addr

I9 I8 I7 I6
a3 a2 a1 a0

At complement on 2 expression −8 to +7

• addr ⊕ K_2 → addr

I7 I6
a1 a0

At complement on 2 expresion −2 to +1

• addr ⊕ K_1 → addr K=+1

During single precision command, 1 word of K (addr) is handled.

$$K_S = -d_{15} + \sum_{i=1}^{15} 2^{-i} d_{15-i}$$

During double precision command, 2 word (32b) of K (addr) and K (addr ⊕ 1) are handled. Here,

$$K_d = -d_{31} + \sum_{i=1}^{31} 2^{-i} d_{31-i}$$

With K (addr) at low word, K (addr ⊕ 1) at high word, 1 increment from the addr specified by the user, (addr ⊕ 1 → addr) execution is completed.
For commands where K-RAM is not handled, the present address remains unchanged.

At the forced 0 address jump every sampling cycle, reset is performed to addr=0.
K-RAM address space is shaped as a ring. (63 ⊕ 1 → 0, 0 ⊕ (−1) → 63).
During Power ON K-RAM contents are not defined.

(2) D-RAM address setting

D-RAM address specify by the user is a logical address and not a physical address.
At the forced 0 address jump every sampling cycle, the ring address counter DAC is incremented by 6 bit.
The logical address addr modulo added to the ring address counter DAC is the physical address that actually points.

Physical addr=DAC⊕addr

What follows is all about logical address addr.

Absolute address specify • $D_{(d)} \rightarrow addr$

I12	I5 I4 I3 I2 I1 I0
H	a5 a4 a3 a2 a1 a0

At absolute expression 0 to 63

Relative address specify • $addr \oplus D_{(r)} \rightarrow addr$

I12	I5 I4 I3 I2 I1 I0
L	a5 a4 a3 a2 a1 a0

At complement on 2 expression −32 to +31

• $addr \oplus D_4 \rightarrow addr$

I3 I2 I1 I0
a3 a2 a1 a0

At complement on 2 expression −8 to +7

• $addr \oplus D_2 \rightarrow addr$

I1 I0
a1 a0

At complement on 2 expression −2 to +1

• $addr \oplus D_+ \rightarrow addr$ $\quad D = +1$

During single precision command, 1 word of D (addr) is handled

$$D_S = -d_{15} + \sum_{i=1}^{15} 2^{-i} d_{15-i}$$

During double precision command, 2 word (32b) of D (addr) and D (addr ⊕ 1) are handled.

$$D_d = -d_{31} + \sum_{i=1}^{31} 2^{-i} d_{31-i}$$

D (addr) is high word and D (addr ⊕ 32) is low word.
When there is no D-RAM address specify command the present address remains unchanged. (addr → addr)

At the forced 0 address jump every sampling cycle, reset is executed to addr=0.
Address space between D-RAM is ring shaped. (63 ⊕ 1 → 0, 0 ⊕ (−1) → 63)
At Power ON, D-RAM contents are undefined.

MPY Command

With the 2 bit of instructions I23 and I22, data length that is input to the multiplicator, is determined. Through this 4 types of MPY mode can be handled. Also, the command execution cycle is regulated by each mode.

I23	I22	bit*bit	Execution cycle
L	L	16 * 16	1
H	H	16 * 32	2
H	L	32 * 16	2
H	H	32 * 32	3

With the 2 bit of instructions I21 and I20, the type of data input to the multiplicator is determined. Here K indicates that the address specified with this command is from K-RAM data. Similarly, D indicates the address specified with this command is from D-RAM data.

I21	I20	type*type
L	L	K * D
H	H	K * X
H	L	X * D
H	H	X * X

X indicates this is the register assigned by the command. It is input to the multiplicator through the main bus.
When X is double precision specified, respective H/L registers are handled in pairs. In this case the resister assigned is handled in high word and the corresponding register in low word.

A more detailed table will turn out as follows.

I21 I20	L L	L H	H L	H H
I23 I22	K * D	K * X	X * D	X * X
L L	K16 *D16	K16 *X16	X16 *D16	X16 *X16
L H	K16 *D32	K16 *X32	X16 *D32	—
H L	K32 *D16	K32 *X16	X32 *D16	—
H H	K32 *D32	K32 *X32	X32 *D32	X32 *X32

For X*X with MPY command, either 16b*16b or 32b*32b is used. However for transfers where double precision X is at the source, X16*X32 type can be used.

Multiplication results enter register P and can be used with the next command.
P bit length is at 33 bit and (−1) * (−1)=+1 can also be stored.

$$P = -2d_{32} + \sum_{i=0}^{31} 2^{-i} d_{31-i} \qquad +1 \geqq P \geqq -1 + 2^{-31}$$

The multiplicator itself operates all the time. P is renewed with every command.
In save commands where there is no X16*X32, X32*X16 or MPY command, P is undefined.

I9	I8	I7	I6	I3	I2	I1	I0	×
L	L	L	L					I 1 H
L	L	L	H					I 1 L
L	L	H	L					I 2 H
L	L	H	H					I 2 L
L	H	L	L					O 1 H
L	H	L	H					O 1 L
L	H	H	L					O 2 H
L	H	H	H					O 2 L
H	L	L	L					D 1 H
H	L	L	H					D 1 L
H	L	H	L					BO 1 H
H	L	H	H					BO 1 L
H	H	L	L					BO 2 H
H	H	L	H					BO 1 L
H	H	H	L					AH
H	H	H	H					AL

AU Command

I19	I18	I17	I16=L	I16=H	Zero	Nz	Plus	Minus	OVF	XOVF
L	L	L	0+P →Acc	0+4P→Acc	○	○	○	○	○	○
L	L	H	Acc+P →Acc	Acc+4P→Acc	×	×	○	○	○	○
L	H	L	0−P →Acc	0−4P→Acc	○	○	○	○	○	○
L	H	H	Acc−P →Acc	Acc−4P→Acc	○	○	○	○	○	○
H	L	L	0+R →Acc	0+4R→Acc	○	○	○	○	○	○
H	L	H	Acc+R →Acc	Acc+4R→Acc	×	×	○	○	○	○
H	H	L	|R| →Acc	|4R| →Acc	○	○	○	○	○	○
H	H	H	Acc−R	Acc−4R	○	○	○	○	○	○

For the 4bit of Instructions I19 to I16 AU command is provided |R |and |4R |are absolute values. 'Acc-R' and 'Acc-4R' are absolute values. 'Acc-R' and 'Acc-4R' are comparison commands. Multiplication results are not stored in Acc, and Acc holds the previous value.

Acc bit length is at 34bit.

$$Acc=-4d_{33}+\sum_{i=-1}^{31} 2^{-i}d_{31-i} \qquad 4-2^{-31} \geqq Acc \geqq -4$$

Min. resolution capability 2^{-31}

P is at 33bit of multiplication results from the previous command. It is code expanded to 34bit for use. R stands at a 32bit value as entered in R register by transfer commands from the commands received up to that. It is similarly code expanded to 34bit for use.

There are 5 Flags for the multiplication results of AU commands to be used when the following command is a conditional jump command. However where X mark is shown on the above chart, it is undefined, so exercise care.

Zero ····· Acc = 0
Non Zero ····· Acc ≠ 0
Plus ····· Acc ≧ 0
Minus ····· Acc < 0
Over Flow ····· Acc ≧1 or Acc<-1

Only for comparison commands Flag is raised for 'Acc-R' and Acc-4R.
XOVF output pin turns to active L during the command in execution after OVF has turned to true.

When Acc value is used for MPY, transfer or barrel shifter, it passes through clipper to be used in 32bit length.
Assuming clipper output=A, we have:

IF Acc ≧ 1 then $A=1-2^{-31}$
else 1 >Acc ≧-1 then A=Acc
else -1>Acc then A=-1

Transfer command

(1) Source and Destination

For the origin (source) of Transfer command K-RAM, D-RAM and X are provided.
Similarly, for the destination of transfer command K-RAM, D-RAM and Y are provided.
Accordingly, K-RAM and Serial I/O output registers (O1H~O2L) can be used as temporary registers.
Combinations are provided as follows.
{K-RAM, D-RAM} → Y
X → Y
X → {K-RAM, D-RAM}
In between RAM there is no direct transfer.

I9	I8	I7	I6	I3	I2	I1	I0	X
L	L	L	L					I1H
L	L	L	H					I1L
L	L	H	L					I2H
L	L	H	H					I2L
L	H	L	L					O1H
L	H	L	H					O1L
L	H	H	L					O2H
L	H	H	H					O2L
H	L	L	L					DIH
H	L	L	H					DIL
H	L	H	L					BO1H
H	L	H	H					BO1L
H	H	L	L					BO2H
H	H	L	H					BO2L
H	H	H	L					AH
H	H	H	H					AL

I9	I8	I7	I6	I3	I2	I1	I0	Y
L	L	L	L					——
L	L	L	H					——
L	L	H	L					RH
L	L	H	H					RL
L	H	L	L					O1H
L	H	L	H					O1L
L	H	H	L					O2H
L	H	H	H					O2L
H	L	L	L					DOH
H	L	L	H					DOL
H	L	H	L					BI1H
H	L	H	H					BI1L
H	H	L	L					BI2H
H	H	L	H					(keep)
H	H	H	L					(keep)
H	H	H	H					(keep)

Even if there is a transfer command to Y, incase it is not actually used, Y assignment uses 0 or 1.
BO1H to BO2L for X and BI1H to BI2H for Y, relate to the barrel shifter and will be referred to later on. X and Y assignment can be set independently for the transfer command of single precision data.
For the transfer command of double precision data, X and Y came in pair as H/L registers. The one assigned is processed as high word register.
Whether the transfer command is of single precision or double precision depends on the transfer origin (source). That is determined through I23 and I22bit of MPY command.
MPY command uses for X*X, 16b*16b (I23, I22=LL, 1 cycle) or 32b*32b (I23, I22=HH, 3 cycle). Should the multiplication be ignored, double precision transfer can be executed at 16b*32b (I23, I22=LH, 2 cycle).

Be careful with 2 the following types of transfer commands that are prohibited.
①Between serial I/O output register of the same register (EX) O1H → O1H
②Respective registers relating to the barrel shifter B2H → B1L

(2) Barrel Shifter

Barrel shifter operation command is inserted in the transfer commands.
There are 3 types of barrel shifter operation commands depending on the transfer destination Y register.

Barrel shifter operaiton command	Transfer destination Y Register	Transfer data (16b) d_{15} d_{14} d_{13} d_{12} d_{11} d_{10} ~ d_0
①Positive value floating-point type conversion	BI1H	— — — — — — ~ —
②Arithmetic left shift	BI1L	— S_3 S_2 S_1 S_0 — ~ —
③Arithmetic right shift	BI2H	— S_3 S_2 S_1 S_0 — ~ —

As a rule those are single precision transfer commands. As for transfer data in the case of ① Positive value floating-point type conversion, anything will do. For ② Arithmetic left shift and ③ Arithmetic right shift the amount of shift S is specified in the 4 bit d_{14} to d_{11}. Conversion scale is, for ① also included, 0 to 15 bit .

$$S=\sum_{i=0}^{3}2^{i}S_i \qquad 15\geqq S\geqq 0$$

Input data to be converted is 31 bit data A^{∇}, excluding LSB, taken from value A (32b) or the result value Acc from the previous command, passed through a clipper.

$$A^{\nabla}=-a_{31}+\sum_{i=1}^{30}2^{-i}a_{31-i} \qquad 1-2^{-30}\geqq A^{\nabla}\geqq -1$$

The converted results can be observed from the following 4 registers. The value is kept until the following barrel shifter operation command is issued.

B01H is the respective data converted value.

$$BO1H=-d_{15}+\sum_{i=1}^{15}2^{-i}d_{15-i}$$

BO1L shows input A with the exclusion of sign bit, where the upper 4 bit are inverted and the rest is filled with zero.

BO2H and BO2L apply a only during floating-point type conversion. The amount of shift Q is included.

$$Q=\sum_{i=0}^{3}2^{i}q_i \qquad 15\geqq Q\geqq 0$$

Output X register	Output data (16b) d_{15} d_{14} d_{13} d_{12} d_{11} d_{10} ~ d_0
BO1H	b_{15} $\overline{b_{14}}$ $\overline{b_{13}}$ $\overline{b_{12}}$ $\overline{b_{11}}$ b_{10} ~ b_0
BO1L	a_{31} $\overline{a_{30}}$ $\overline{a_{29}}$ $\overline{a_{28}}$ $\overline{a_{27}}$ 0 ~ 0
BO2H	0 q_3 q_2 q_1 q_0 0 ~ 0
BO2L	0 0 q_3 q_2 q_1 0 ~ 0

① Positive value floating-point type conversion

Positive value A^{∇} ($\geqq 0$, $a_{31}=0$) is converted to floating-point type ($A^{\nabla} \approx BO1H \cdot 2^{-Q}$).

Case I $A^{\nabla} \geqq 2^{-16}$

$$A^{\nabla} = -0+\sum_{i=1}^{30} 2^{-i}a_{31-i} \quad \text{for} \quad 15 \geqq Q \geqq 0,\ a_{31-(Q+1)}=1$$

$$= \{\sum_{i=1}^{30-Q} 2^{-i}a_{31-Q-i}\} \cdot 2^{-Q} \approx \{-0+\sum_{i=1}^{15} 2^{-i}a_{31-Q-i}\} \cdot 2^{-Q} = BO1H \cdot 2^{-Q}$$

This, to turn into the regular form $BO1H \geqq \frac{1}{2}$ ($b_{14}=1$)

Case II $2^{-16} > A^{\nabla}$

$$A^{\nabla} = -0+\sum_{i=1}^{30} 2^{-i}a_{31-i} = \sum_{i=17}^{30} 2^{-i}a_{31-i} = \{-0+\sum_{i=2}^{15} 2^{-i}a_{16-i}\} \cdot 2^{-15} = BO1H \cdot 2^{-Q}$$

This becomes $\frac{1}{2} > BO1H$ ($d_{14}=0$), $Q=15$

② Arithmetic left shift

With sign bit fixed, S bit of A^{∇} is shifted left

$$O1H = -a_{31}+\sum_{i=1}^{15} 2^{-i}a_{31-S-i}$$

Case I $2^{-S} > A^{\nabla} \geqq 0$

$$A^{\nabla} \cdot 2^{S} = \{-0+\sum_{i=1}^{30} 2^{-i}a_{31-i}\} \cdot 2^{S} = \{\sum_{i=S+1}^{30} 2^{-i}a_{31-i}\} \cdot 2^{S} = \sum_{i=1}^{30-S} 2^{-i}a_{31-S-i}$$

$$\approx -0+\sum_{i=1}^{15} 2^{-i}a_{31-S-i} = BO1H$$

Case II $0 > A^{\nabla} \geqq -2^{-S}$

$$A^{\nabla} \cdot 2^{S} = \{-1+\sum_{i=1}^{30} 2^{-i}a_{31-i}\} \cdot 2^{S} = -\{\sum_{i=1}^{30} 2^{-i}\overline{a_{31-i}}+2^{-30}\} \cdot 2^{S}$$

$$= -\{\sum_{i=S+1}^{30} 2^{-i}\overline{a_{31-i}}+2^{-30}\} 2^{S} = -\{\sum_{i=1}^{30-S} 2^{-i}\overline{a_{31-S-i}}+2^{-(30-S)}\}$$

$$= -1+\sum_{i=1}^{30-S} 2^{-i}a_{31-S-i} \approx -1+\sum_{i=1}^{15} 2^{-i}a_{31-S-i} = BO1H$$

Case III $A^{\nabla} \geqq 2^{-S}$ or $-2^{-S} > A^{\nabla}$

In this case conversion cannot be executed correctly

③ Arithmetic right shift
With sign bit fixed, S bit of A^{∇} is shifted right.

$$BO1H = -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{15} 2^{-i} a_{31+S-i}$$

However,

$$S = 0 \quad BO1H = -a_{31} + \sum_{i=1}^{15} 2^{-i} a_{31-i} \approx A^{\nabla}$$

$$S = 15 \quad BO1H = -a_{31} + \sum_{i=1}^{15} 2^{-i} a_{31} = -2^{-15} a_{31}$$

$$A^{\nabla} \cdot 2^{-S} = \{-a_{31} + \sum_{i=1}^{30} 2^{-i} a_{31-i}\} \cdot 2^{-S} = -2^{-S} a_{31} + \sum_{i=1}^{30} 2^{-S-i} a_{31-i}$$

$$= -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{30+S} 2^{-i} a_{31+S-i}$$

$$\approx -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{15} 2^{-i} a_{31+S-i} = BO1H$$

Flag BSQ

This flag is renewed with every barrel shifter operation command. This applies only during positive floating-point conversion.
When positive value floating-point conversion is executed, from that bit shift Q

$$Q = \sum_{i=0}^{3} 2^{i} q_i$$

q_0 becomes the Flag BSQ.
That flag value is kept until the following barrel shifter operation command comes.
When condition jump command and barrel shifter operation command are on the same command, Flag BSQ that is utilized for condition jump, is the flag value of the previous barrel shifter operation command.

BSQ=ON The bit shift amount of the positive value floating-point conversion is an odd number
BSQ=OFF The bit shift amount of the positive value floating-point conversion is an even number

Jump system command

Jump commands for the instruction address include: conditional jump, unconditional jump and sub routine call. They all jump to addresses expressed in 6bit and containing an A.

$$A=\sum_{i=0}^{5} 2^i A_i \qquad 63 \geqq A \geqq 0$$

A5	A4	A3	A2	A1	A0
I5	I4	I3	I2	I1	I0
I5	I4	I3	I2	I11	I10
I5	I4	I9	I8	I11	I10

Sub routine call and loop jump can stack instruction address. They are formed by a 2-address FILO and can execute up to a double conbination. When stack performs a forced 0 address jump, it also keeps the previous condition.

(1) Conditional jump JP(F)

I15	I14	I13
H	H	H

When the condition is met, the following command executes the command of the address ahead of the jump.
When the condition is not met, the command after that executes the command of the address in the order.

I12	I11	I10	Flag	Conditions
L	L	L	Zero	Results of previous commands Acc=0
L	L	H	Non zero	Results of previous commands Acc=0
L	H	L	Plus	Results of previous commands Acc≧0
L	H	H	Minus	Results of previous commands Acc<0
H	L	L	Over flow	Results of previous commands Acc≧1 or Acc<−1
H	L	H	BSQ	Barrel shifter operation command (positive value floating-point type conversion) up to the previous command is odd numbered shift bit
H	H	L	(keep)	Actually same value as unconditional jump
H	H	H	(keep)	

* Below zero and Non zero cannot be used

Acc+P →Acc Acc+4P→Acc
Acc+R →Acc Acc+4R→Acc

(2) Non conditional jump JMP

I15	I14	I13	I12
H	L	H	L
H	H	L	L

Elements from this command, execute the command of the address ahead of the jump, unconditionally

(3) Sub routine call CAL

I15	I14	I13	I12
H	L	H	H
H	H	L	H

This command executes the command of address ahead of the jump for the sub routine. Also it pushes to the stack the address following this command.

Return RTN

I15	I11	I10
I15	I5	I4
L	H	L

Next this command pops out the address from the stack and executes the command of that address.

(4) Loop jump

Sets the number of loops (0 to 15) in the 4 bit loop counter to repeatedly execute a certain group of commands (1 to 16 times).

Loop counter set
LCS (C)

I15 I14 I13	I12	I11 I10 I5 I4
H L L	L	C_3 C_2 C_1 C_0

Number of loops

$C=\sum_{i=0}^{3} 2^{-i} C_i \quad 15 \geqq C \geqq 0$

Sets the number of loops in the loop counter

Loop counter and loop address set
LTS (C)

I15 I14 I13	I12	I11 I10 I5 I4
H L L	H	C_3 C_2 C_1 C_0

Number of loops

$C=\sum_{i=0}^{3} 2^{-i} C_i \quad 15 \geqq C \geqq 0$

Sets the number of loops in the loop counter and also pushes into the stack the next instruction address (loop head address)

Loop address set
LPS

I15	I11 I10 I5 I4
L	H H

Pushes the next instruction address (loop head address) into the next instruction address

Loop jump
LPJ

I15	I11 I10 I5 I4
L	L H

Decrements the loop counter value
① C≧0 jumps to the address in the stack
② C<0 Pops out the stack and proceeds in order to the command of the following address

Example)

Program	Execution
LTS (1)	LTS 1→C
Command group A	Command group A
LPJ	LPJ C-1= 0→C (≧0)
Command group B	Command group A
	LPJ C-1= −1→C (<0)
	Command group B

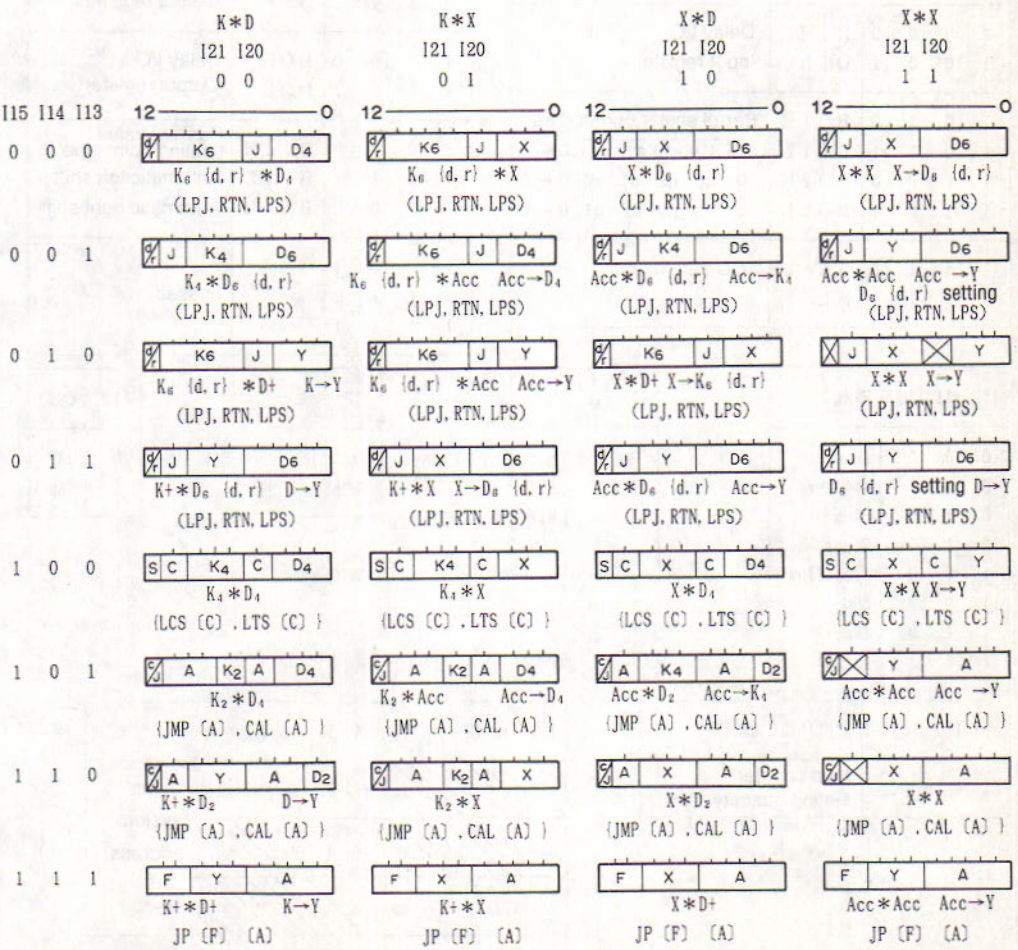
The stack has a double structure. Accordingly, the following can be executed.

- The subroutine inside the subroutine
- The loop jump inside the sub routine
- The subroutine inside the loop jump

The loop jump inside the loop jump cannot be executed

Execution command and machine language

I23	I22		I21	I20		I19	I18	I17	I16=0	I16=1
0	0	16*16	0	0	K*D	0	0	0	0+P	0+4P
0	1	16*32	0	1	K*X	0	0	1	Acc+P	Acc+4P
1	0	32*16	1	0	X*D	0	1	0	0−P	0−4P
1	1	32*32	1	1	X*X	0	1	1	Acc−P	Acc−4P
						1	0	0	0+R	0+4R
						1	0	1	Acc+R	Acc+4R
						1	1	0	|R|	|4R|
						1	1	1	Acc−R	Acc−4R ····· Acc Without latching



I9 I8 I7 I6 / I3 I2 I1 I0	X	
0 0 0 0	I 1 H	Serial I/O CH1
0 0 0 1	I 1 L	Input register
0 0 1 0	I 2 H	Serial I/O CH2
0 0 1 1	I 2 L	Input register
0 1 0 0	O 1 H	Serial I/O CH1
0 1 0 1	O 1 L	Output register
0 1 1 0	O 2 H	Serial I/O CH2
0 1 1 1	O 2 L	Output register
1 0 0 0	D I H	Delay I/O
1 0 0 1	D I L	Input register
1 0 1 0	BO 1 H	Barrel shifter output data
1 0 1 1	BO 1 L	a15 $\overline{a14}$ $\overline{a13}$ $\overline{a12}$ $\overline{a11}$ 0 — 0
1 1 0 0	BO 2 H	0 q3 q2 q1 q0 0 — 0
1 1 0 1	BO 2 L	0 0 q3 q2 q1 0 — 0
1 1 1 0	AH	ACC data output
1 1 1 1	AL	

I9 I8 I7 I6 / I3 I2 I1 I0	Y	
0 0 0 0	——	Assignment when transfer command is not to be given
0 0 0 1	——	
0 0 1 0	RH	R register
0 0 1 1	RL	
0 1 0 0	O 1 H	Serial I/O CH1
0 1 0 1	O 1 L	Output register
0 1 1 0	O 2 H	Serial I/O CH2
0 1 1 1	O 2 L	Output register
1 0 0 0	DOH	Delay I/O
1 0 0 1	DOL	Output register
1 0 1 0	B I 1 H	Positive value floating point type
1 0 1 1	B I 1 L	Arithmetic left shift
1 1 0 0	B I 2 H	Arithmetic right shift
1 1 0 1	(keep)	unused
1 1 1 0	(keep)	
1 1 1 1	(keep)	

I12 I11 I10	Flag
0 0 0	Zero
0 0 1	Non zero
0 1 0	Plus
0 1 1	Minus
1 0 0	Over flow
1 0 1	BSQ
1 1 0	(keep)
1 1 1	(keep)

I11 I10	J
0 0	none
0 1	LPJ
1 0	RTN
1 1	LPS

I12	S
0	LCS
1	LTS

I12	C/J
0	JAP
1	CAL

I11 I10 I5 I4	C (15≧C ≧0)
C_3 C_2 C_1 C_0	loop counter setting quantity

I11 I10 I9 I8 I5 I4 I3 I2 I1 I0	
a_5 a_4 a_3 a_2 a_1 a_0	Jump system address 0~63
a_1 a_0 a_5 a_4 a_3 a_2	
a_1 a_0 a_3 a_2 a_5 a_4	

K	I12 I11 I10 I9 I8 I7 I6	address
$K_6(d)$	1 R_5 R_4 R_3 R_2 R_1 R_0	0 to 63
$K_6(r)$	0 R_5 R_4 R_3 R_2 R_1 R_0	−32 to +31
K_4	R_3 R_2 R_1 R_0	−8 to +7
K_2	R_1 R_0	−2 to +1
K_+		+1

D	I12 I11 I10 I9 I8 I7 I6	address
$D_6(d)$	1 d_5 d_4 d_3 d_2 d_1 d_0	0 to 63
$D_6(r)$	0 d_5 d_4 d_3 d_2 d_1 d_0	−32 to +31
D_4	d_3 d_2 d_1 d_0	−8 to +7
D_2	d_1 d_0	−2 to +1
D_+		+1

Points on Execution Commands

Execution cycle

A command can be repeatedly executed from the command 0 address by means of the forced 0 address jump every Serial I/O sampling cycle.

Now, Assume that from the time 0 address has started, up until just before 0 address jump the number of cycles is N. [Cycle 0 to cycle (N-1)]

① Cycle 0 to cycle (N-3) ..... Normal cycle: Execution possible
② Cycle (N-2) ..... KSL cycle: with the exception of K-RAM access, execution possible
③ Cycle (N-1) ..... KSH cycle: Execution impossible (Any command will do)

* To provide time for K-RAM, I-RAM and the micro computer to interface ② and ③ are available.

The number of cycles N is given through the following formula, with fs for sampling frequency and fkck as cycle clock frequency.

$$\frac{fkck}{fs} - 1 < N < \frac{fkck}{fs} + 1 \qquad \text{for } fkck = \frac{1}{2} f_{ACK} = \begin{cases} \frac{1}{2} f_{MCK1} \\ \frac{1}{2} f_{MCK2} \end{cases}$$

If fkck is a whole number N=fkck/fs=N1. Cycle 0 to cycle (N_1-1)
If fkck is not a whole number there are 2 cycle patterns

$$N = \begin{cases} N_1, \text{ Cycle 0 to Cycle } (N_1-1) \\ N_1+1, \text{ Cycle 0 to Cycle } N_1 \end{cases}$$

General expression	N	Cycle 0 to cycle (N-3) Normal cycle	Cycle (N-2) KSL cycle	Cycle (N-1) KSH cycle
fkck/fs whole number	$N=N_1$	Cycle 0 to cycle (N_1-3)	Cycle (N_1-2)	Cycle (N_1-1)
fkck/fs is not a whole number	$N=N_1$ N_1+1	Cycle 0 to cycle (N_1-3) Cycle 0 to cycle (N_1-2)	Cycle (N_1-2) Cycle (N_1-1)	Cycle (N_1-1) Cycle N_1

Therefore when fkck/fs is a whole number

① Cycle 0 to cycle (N_1-3)	Normal cycle:	Execution possible
② Cycle (N_1-2)	KSL cycle:	with the exception of K-RAM access, execution possible
③ Cycle (N_1-1)	KSH cycle:	Execution impossible (Any command will do)

Or when fkck/fs is not a whole number

A Cycle 0 to cycle (N_1-3)	: Execution always possible at normal cycle.
B cycle (N_1-2)	: Turns into normal cycle or KSL cycle. Execution possible with the exception of K-RAM
C cycle (N_1-1)	: Turns into KSL cycle or KSH cycle. A command that does not use transfer command. (In fact, execution impossible)
D cycle N_1	: Turns into KSH cycle or does not exist. Execution impossible (Any command will do)

Example 1) When fkck=6.144 MHz fs=48 KHz

$$\frac{fkck}{fs}=128 \quad \therefore N=N_1=128 \text{ Cycle 0 to cycle 127}$$

$$\therefore \begin{cases} ① \text{ Cycle 0 to 125} \\ ② \text{ Cycle 126} \\ ③ \text{ Cycle 127} \end{cases}$$

Example 2) When fkck=6.144 MHz fs=44.1 KHz

$$\frac{fkck}{fs}=139.3... \quad \therefore N=\begin{cases} N_1 = 139 \text{ cycle 0 to cycle 138} \\ N_1+1 = 140 \text{ cycle 0 to cycle 139} \end{cases}$$

$$\therefore \begin{cases} \text{A Cycle 0 to cycle 136} \\ \text{B Cycle 137} \\ \text{C Cycle 138} \\ \text{D Cycle 139} \end{cases}$$

Serial I/O and Register

(1) Serial I/O input register

The conditions for transfers with serial I/O input register as source or for cycle n without MPY are:

$$N-4\frac{1}{4} < n < N-2\frac{3}{4}+M$$ SIN delay from M ··· BCK falling edge

As $M=2\frac{3}{4}$ (fKCK)

$$N-4\frac{1}{4} < n < N \quad \therefore N-4 \leqq n \leqq N-1$$

- $\frac{fKCK}{fS}$ = for whole number $n = \{N-4 \leqq n \leqq N-1\} = \{N_1-4 \leqq n \leqq N_1-1\}$

Cycle 0 to cycle (N_1-5)	Serial input data transferred to the previous sampling space is in this space register and can be handled freely.
Cycle (N_1-4) to cycle (N_1-1)	In this space usage of serial I/O input register is prohibited.

* In certain cases cycle (N_1-2) can be used. Check when necessary.

- $\frac{fKCK}{fS}$ = for whole number $n = \{N-4 \leqq n \leqq N-1\} = \{N_1-4 \leqq n \leqq N_1\}$

Cycle 0 to cycle (N_1-5)	Serial input data transferred to the previous sampling space is in this space register and can be handled freely.
Cycle (N_1-4) to cycle N_1	In this space usage of serial I/O input register is prohibited.

(2) Serial I/O output register

Cycle n conditions for transfers that can not be executed with serial I/O output register as destination

$$N-4\frac{1}{4}+\frac{fKCK}{fB}-M<n<N-2\frac{3}{4}+\frac{fKCK}{fB}$$ fB ... bit clock frequency

M is a delay margin to be ignored here $N-4\frac{1}{4}+\frac{fKCK}{fB} < n < N-2\frac{3}{4}+\frac{fKCK}{fB}$

24 bit clock system

$$N-4\frac{1}{4}+\frac{1}{48}\frac{fKCK}{fS} < n < N-2\frac{3}{4}+\frac{1}{48}\frac{fKCK}{fS}$$

32 bit clock system

$$N-4\frac{1}{4}+\frac{1}{64}\frac{fKCK}{fS} < n < N-2\frac{3}{4}+\frac{1}{64}\frac{fKCK}{fS}$$

* As no margin is taken for the left side, in certain cases prohibited cycles are not included. Check when necessary.

Example 1) f_{CK}=6.44 MHz fs=48 KHz N=N_1=128 (Cycle 0 to cycle 127)

Serial I/O input register $n = \{N_1-4 \leqq n \leqq N_1-1\} = \{124 \leqq n \leqq 127\}$

$\therefore$ { Cycle 0 to cycle 123 ..... usable
Cycle 124 to cycle 127 ..... unusable

Serial I/O output register 24 clock system $N-4\frac{1}{4}+\frac{1}{48}128 < n < N-2\frac{3}{4}+\frac{1}{48}128$

$$N-1\frac{7}{12} < n < N-\frac{1}{12}$$

$$N-1 \leqq n \leqq N-1$$

$n=N-1=N_1-1=127$

$\therefore$ { Cycle 0 to cycle 126 ..... usable
Cycle 127 ..... unusable

Serial I/O output register 32 clock system $N-4\frac{1}{4}+\frac{1}{64}128 < n < N-2\frac{3}{4}+\frac{1}{64}128$

$$N-2\frac{1}{4} < n < N-\frac{3}{4}$$

$$N-2 \leqq n \leqq N-1$$

$n = \{N-2 \leqq n \leqq N-1\} = \{N_1-2 \leqq n \leqq N_1-1\} = \{126 \leqq n \leqq 127\}$

$\therefore$ { Cycle 0 to cycle 125 ..... usable
Cycle 126 to cycle 127 ..... unusable

Example 2) f_{KCK}=6.144 MHz fs=44.1 KHz $N=\begin{cases} N_1 = 139 \text{ (Cycle 0 to cycle 138)} \\ N_1+1 = 140 \text{ (Cycle 0 to cycle 139)} \end{cases}$

Serial I/O input register $n=\{N_1-4 \leqq n \leqq N_1\} = \{135 \leqq n \leqq 139\}$

$\therefore$ { Cycle 0 to cycle 134 ..... usable
Cycle 135 to cycle 139 ..... unusable

Serial I/O output register 24 clock system $N-4\frac{1}{4}+\frac{1}{48}(139.3...)<n<N-2\frac{3}{4}+\frac{1}{48}(139.3...)$

$$N-1.3... < n < N+0.1...$$

$$n=\{N-1.0\} = \{N_1-1, N_1.0\} = \{138, 139.0\}$$

$\therefore$ { Cycle 1 to cycle 137 ..... usable
Cycle 137, 139, cycle 0 ..... unusable

Serial I/O output register 32 clock system $N-4\frac{1}{4}+\frac{1}{64}(139.3...)<n<N-2\frac{3}{4}+\frac{1}{64}(139.3...)$

$$N-2.0... < n < N-0.5...$$

$$N-2 \leqq n \leqq N-1$$

$$n=\{N-2, N-1\} = \{N_1-2, N_1-1, N_1\} = \{137, 138, 139\}$$

$\therefore$ { Cycle 0 to cycle 136 ..... usable
Cycle 137 to cycle 139 ..... unusable

Delay I/O (Serial mode) and register

(1) Delay I/O input register

Delay I/O input register is input twice during 1 sampling period. For one of those 2 instances the timing is the same as for serial I/O. For the other instance the conditions for the transfer with this register as source or the cycle n when MPY cannot be executed are:

$$\frac{1}{2}\frac{f_{KCK}}{fS}-4\frac{1}{4}<n<\frac{1}{2}\frac{f_{KCK}}{fS}-2\frac{3}{4}+M$$

as $M=\frac{1}{2}\{KCK\}$

$$\frac{1}{2}\frac{f_{KCK}}{fS}-4\frac{1}{4}<n<\frac{1}{2}\frac{f_{KCK}}{fS}-2\frac{1}{4}$$

accordingly $n_2=\{\max n : n<\frac{1}{2}\frac{f_{KCK}}{fS}-4\frac{1}{4}\}$

Cycle 0 to cycle n_2	data transferred during LRCK L level of the previous sampling level is in the register and can be handled freely.
Cycle (n_2+1), cycle (N_2+2)	Usage prohibit cycle
Cycle (n_2+3) to cycle (N_1-5)	data transferred during LRCK H level of the present sampling period is in the register and can be handled freely
Cycle (N_1-4) to cycle (N_1-1)	Usage prohibit cycle

*In certain cases cycle (n_2+3) also becomes usage prohibit cycle. Please check when necessary.

(2) Delay I/O output register

Delay I/O output register outputs twice during 1 sampling period. For one of those 2 instances the timing is the same as for serial I/O. For the other instance, the conditions for cycle n where transfer with this register as destination can not be executed are

$$\frac{1}{2}\frac{fKCK}{fS}-4\frac{1}{4}+\frac{fKCK}{fB}-M<n<\frac{1}{2}\frac{fKCK}{fS}-2\frac{3}{4}+\frac{fKCK}{fB}$$

as M=0 [KCK]

$$\frac{1}{2}\frac{fKCK}{fS}-4\frac{1}{4}+\frac{fKCK}{fB}<n\frac{1}{2}\frac{fKCK}{fS}-2\frac{3}{4}+\frac{fKCK}{fB}$$

24 bit clock system

$$\frac{25}{48}\frac{fKCK}{fS}-4\frac{1}{4}<n<\frac{25}{48}\frac{fKCK}{fS}-2\frac{3}{4}$$

32 bit clock system

$$\frac{33}{64}\frac{fKCK}{fS}-4\frac{1}{4}<n<\frac{33}{64}\frac{fKCK}{fS}-2\frac{3}{4}$$

*In certain cases, as the left side margin is not included, cycles that become prohibited are not included. Please check when necessary.

Example 1) f_{KCK}=6.144 MHz fs=48 kHz N-N_1=128 (Cycle 0 to cycle 127)

Delay I/O input register $n_2<\frac{1}{2}\ 128-4\frac{1}{4}=60-\frac{1}{4}$ $\therefore n_2=59$

$\therefore$
- Cycle 0 to cycle 59 ..... usable
- Cycle 60 to cycle 61 ..... unusable
- Cycle 62 to cycle 123 ..... usable
- Cycle 124 to cycle 127 ..... unusable

Delay I/O output register 24 clock system $\frac{25}{48}\ 128-4\frac{1}{4}<n<\frac{25}{48}\ 128-2\frac{3}{4}$

$$62\frac{5}{12}<n<63\frac{11}{12}$$

N=63

$\therefore$
- Cycle 0 to cycle 62 ..... usable
- Cycle 63 ..... unusable
- Cycle 64 to cycle 126 ..... usable
- Cycle 127 ..... unusable

Delay I/O output register 32 clock system $\frac{33}{64}\ 128\text{-}4\frac{1}{4} < n < \frac{33}{64}\ 128\text{-}2\frac{3}{4}$

$$61\frac{3}{4} < n < 63\frac{1}{4} \qquad n = \{62, 63\}$$

$\therefore$
- Cycle 0 to cycle 61 ..... usable
- Cycle 62 to cycle 63 ..... unusable
- Cycle 64 to cycle 125 ..... usable
- Cycle 126 to cycle 127 ..... unusable

Example 2) f_{XCK}=6.144 MHz fs=44.1 KHz $N = N_1 = 139$ (Cycle 0 to cycle 138) $N_1+1 = 140$ (Cycle 0 to cycle 139)

Delay I/O input register $n_2 < \frac{1}{2}\ 139.3\ldots\text{-}4\ \frac{1}{4} = 65.4\ldots \quad \therefore n=65$

$\therefore$
- Cycle 0 to cycle 65 ..... usable
- Cycle 66 to cycle 67 ..... unusable
- Cycle 68 to cycle 134 ..... usable
- Cycle 135 to cycle 139 ..... usable

Delay I/O output register 24 clock system $\frac{25}{48}\ 139.3\ldots\text{-}4\ \frac{1}{4} < n < \frac{25}{48} 139.3\ldots\text{-}2\frac{3}{4}$

$$68.3\ldots < n < 69.8\ldots \quad . \qquad n=69$$

- Cycle 1 to cycle 68 ..... usable
- Cycle 69 ..... unusable
- Cycle 70 to cycle 137 ..... usable
- Cycle 138 to cycle 0 ..... unusable

Delay I/O output register 32 clock system $\frac{33}{64}\ 139.3\ldots\text{-}4\ \frac{1}{4} < n < \frac{33}{64} 139.3\ldots\text{-}2\frac{3}{4}$

$$67.5\ldots < n < 69.0\ldots \qquad n = \{68, 69\}$$

- Cycle 0 to cycle 67 ..... usable
- Cycle 68 to cycle 69 ..... unusable
- Cycle 70 to cycle 136 ..... usable
- Cycle 137 to cycle 139 ..... unusable

Delay I/O (delay mode) and register

(1) 32 bit delay mode
32 bit Conditions where delay mode can be realized

$$fS \leq \frac{1}{136} fKCK \quad \text{that is} \quad N_1 \geq 136$$

The relation between data to write in DO register and data to read from DI register is.

- DO register
  - Cycle 0 to cycle 66 : data written last in this period is set as CH1 (n)
  - Cycle 67 : write prohibit
  - Cycle 68 to cycle (N_1-2) : data written last in this period is set as CH2 (n)
  - Cycle (N_1-1), (N_1) : write prohibit

- DI register
  - Previous cycle 134 to cycle (N_1-2), cycle 0 to cycle 65 : In this period CH1 data (n-r) can read
  - Cycle 62 to cycle 125 : In this period CH2 data (n-r) can read.
  - Cycle (N_1-1), (N_1) : read prohibit

(2) 30 bit delay mode
30 bit Conditions where delay mode can be realized

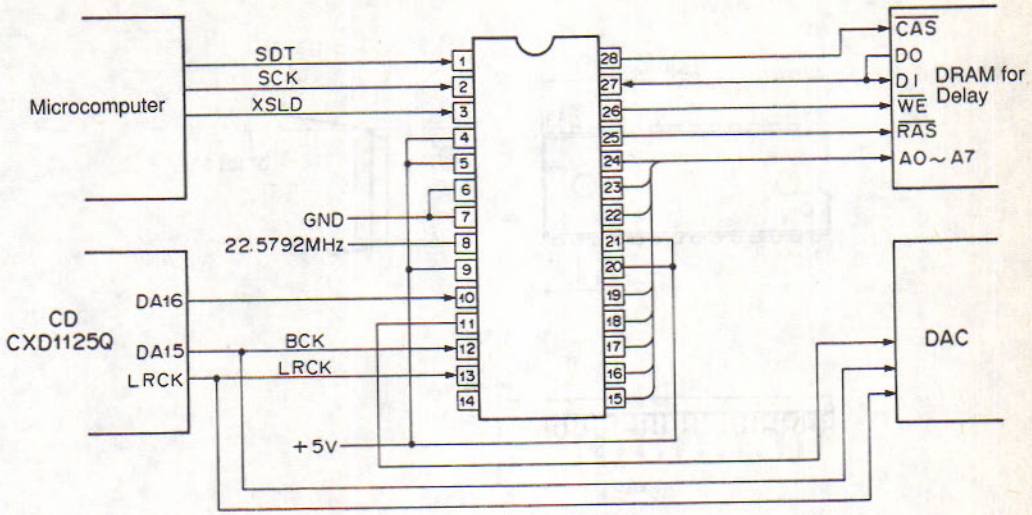
$$fS \leq \frac{1}{128} fKCK \quad \text{that is} \quad N_1 \geq 128$$

The relation between data to write in DO register and data to read from DI register is.

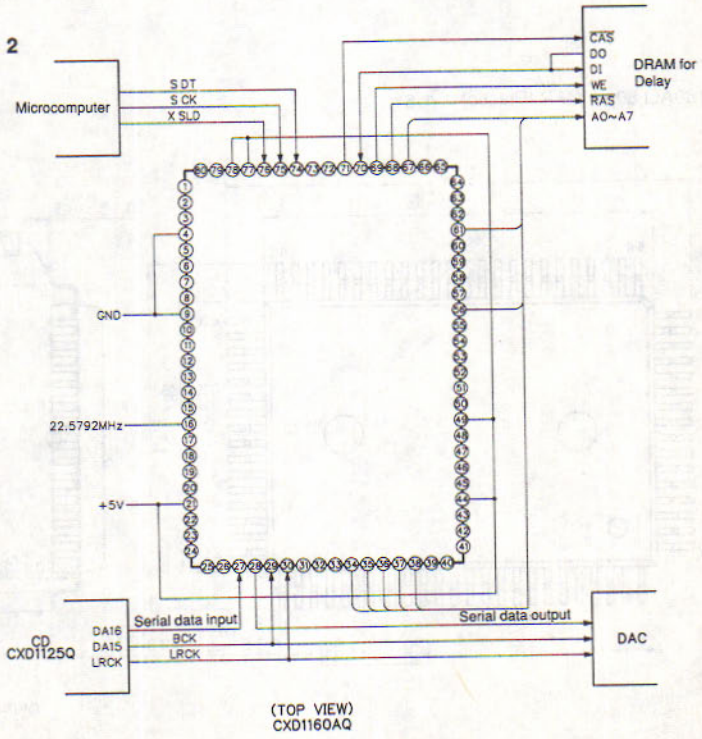
- DO register
  - Cycle 0 to cycle 62 : data written last in this period is set as CH1 (n)
  - Cycle 63 : write prohibit
  - Cycle 64 to cycle (N_1-2) : data written last in this period is set as CH2 (n)
  - Cycle (N_1-1), (N_1) : write prohibit

- DI register
  - Previous cycle 126 to cycle (N_1-2), cycle 0 to cycle 61 : In this period CH1 data (n-r) can read
  - Cycle 62 to cycle 125 : In this period CH2 data (n-r) can read.
  - Cycle (N_1-1), (N_1) : read prohibit

Application example 1

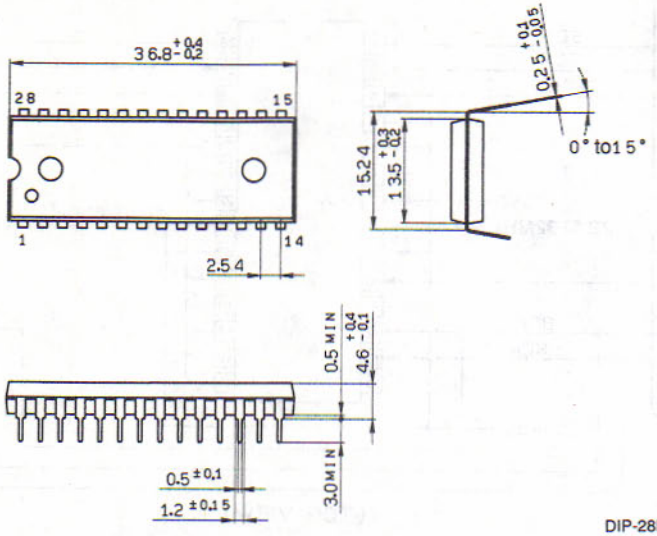


Application example 2



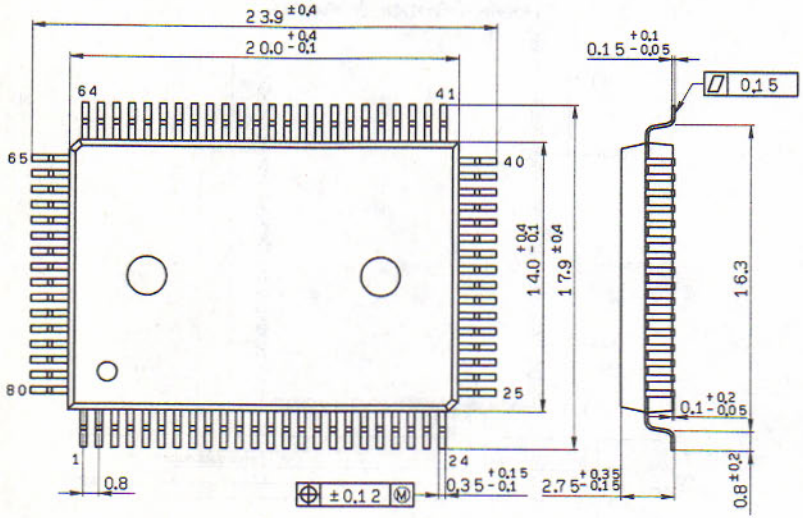
Package Outline Unit: mm

CXD1160AP 28pin DIP (Plastic) 600 mil 4.2 g



DIP-28P-04

CXD1160AQ 80pin QFP (Plastic) 1.6 g



QFP-80P-L01

SONY

CXD1355AQ

Audio Digital Signal Processing LSI with Built-in Digital Filter

Description

The CXD1355AQ is an ADSP (Audio Digital Signal Processor) LSI incorporating an audio digital signal processor with programmable DSP features and an 8-times oversampling filter.

Features

Software programmable digital signal processing features (1/2)×fs down-sampling with post processing using 64-times multiply/add operations possible.

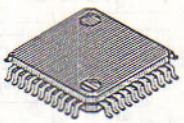
Through the use of external delay DRAM (64k×4-bit/256k×4-bit selectable), sound field processing attributes such as delay, echo and reverberation can be controlled. By cascading the internal filters–107th, 19th, and 3rd FIR filters–8-times or 4-times oversampling filters is possible.

In addition this LSI incorporates attenuator functions and a host of other features into a single chip solution for enhancing the performance of audio systems.

Functions

- Programmable sound field processing, pre-processing down-sampling (fs→fs/2), and post-processing up-sampling (fs/2→fs).
- External delay RAM, 64k×4bit or 256k×4bit.
- Internal coefficient RAM for DSP functions and command RAM.
- Delays up to a maximum of 64k samples for both L and R channels.
- Built-in 2-channel oversampling digital filters for handling 8-times/4-times oversampling.
- Filter characteristics
  Ripple : ± 0.001 dB or less (0 to 20kHz)
  Attenuation : –70 dB or less (24.1 to 150kHz)
- Digital de-emphasis function
- Digital attenuation function
- Built-in 1st-order noise shaper
- Digital offset (+1%) function
- Input data inversion
- I/O format
  Input : 2's complement MSB first serial (16-bit slot)
  Output : 2's complement MSB first serial (16-bit or 18-bit slot selectable)

44 pin QFP (Plastic)



Structure

Silicon gate CMOS

Absolute Maximum Ratings

(Ta=25°C, Vss=0V)

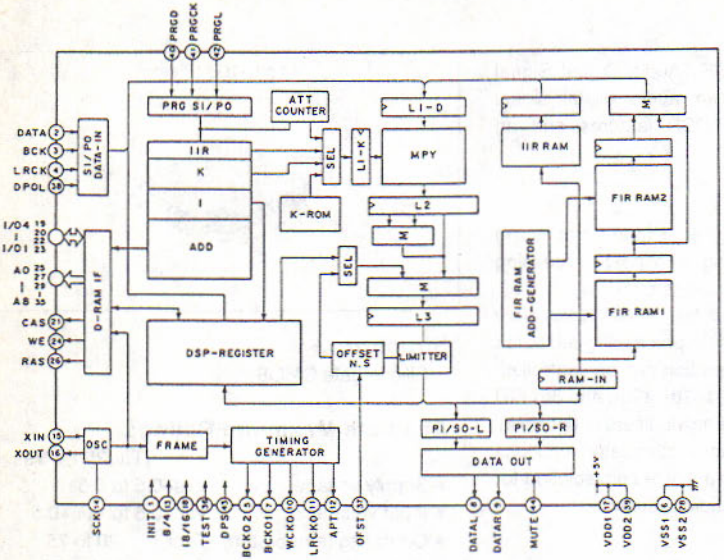
• Supply voltage	V_{DD}	Vss–0.5 to 6.5	V
• Input voltage	V_I	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to 75	°C
• Storage temperature	Tstg	–55 to 150	°C

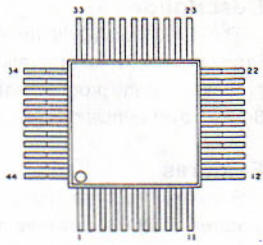
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (Typ. 5.0)	V
• Operating temperature	Topr	–20 to 75	°C
• OSC frequency	f_{XT}	10 to 20	MHz

E92137 – ST

Block Diagram and Pin Configuration (Top View)





Pin Description

Pin No.	Symbol	I/O	Description
1	INIT	I	Initialize. Active when set "L". Re-synchronized by the rising edge of this signal.
2	DATA	I	1 sampling, 2-channel serial data input. Data is in 2's complement MSB first format.
3	BCK	I	Serial data input for serial bit clock. Serial input data is latched by the rising edge of this signal.
4	LRCK	I	Serial I/O for the sampling frequency clock input. "L": Channel 2 data transfer active; "H": Channel 1 data transfer active.
5	BCKO2	O	Bit clock output with weak-output signal of 192fs frequency.
6	Vss1	——	GND
7	BCKO1	O	Bit clock output. 192fs frequency.
8	DATA L	O	Serial data output. Data format is 2's complement MSB first. 8fs mode: L channel output. 4fs mode: L channel + R channel output.
9	DATA R	O	Serial data output. Data format is 2's complement MSB first. 8fs mode: R channel output. 4fs mode: rnade active by setting to "L".
10	WCKO	O	Word clock output of serial data.
11	LRCKO	O	Serial data sampling frequency clock output.
12	APT	O	Aperture clock output.
13	8/4	I	8fs/4fs input select. "H": 8fs; "L": 4fs.
14	SCK	O	System clock output. fsck=fxt=384fs.
15	X OUT	O	Liquid crystal display oscillation circuit output.

Pin No.	Symbol	I/O	Description
16	X IN	O	Liquid crystal display oscillation circuit input. fxt = 384fs.
17	$V_{DD}1$	——	Power supply (+5 V)
18	18/16	I	Input for selecting output data bit-length. "H": 18-bit; "L": 16-bit.
19	I/O1	I/O	External DRAM data I/O1.
20	I/O2	I/O	External DRAM data I/O2.
21	CAS	O	External DRAM column address strobe output.
22	I/O3	I/O	External DRAM data I/O3.
23	I/O4	I/O	External DRAM data I/O4.
24	WE	O	External DRAM write-enable output. Active when set "L".
25	A0	O	External DRAM address output A0.
26	RAS	O	External DRAM low-address strobe output.
27	A1	O	External DRAM address output A1.
28	Vss2	——	GND
29	A2	O	External DRAM address output A2.
30	A3	O	External DRAM address output A3.
31	A4	O	External DRAM address output A4.
32	A5	O	External DRAM address output A5.
33	A6	O	External DRAM address output A6.
34	A7	O	External DRAM address output A7.
35	A8	O	External DRAM address output A8.
36	TEST	I	Test pin. Fixed at GND in normal operation mode.
37	OFST	I	Offset select input. "H": offset; "L": non-offset.
38	DPOL	I	Input data for inverted/non-inverted select. "H": inverted; "L": non-inverted.
39	$V_{DD}2$	——	Power supply (+5V)
40	PRGD	I	Serial data input for receiving instructions, coefficients, and operators transferred from the microprocessor.
41	PRGCK	I	Serial clock input for PRGD. Data is latched by the rising edge of this signal.
42	PRGL	I	Latch input for internally latching serial data set from the microprocessor. Active when set "L".
43	DSP	I	Input select for DSP operations. "H": DSP ON; "L": DSP OFF.
44	MUTE	I	Mute input. Active when set "H".

Input Capacity

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin *1	C_{IN}			3	5	pF
Input pin *2	C_{IN}	Input mode		4	6	pF

*1 All pins except for the I/O.
*2 I/O pin

Electrical Characteristics
DC Characteristics

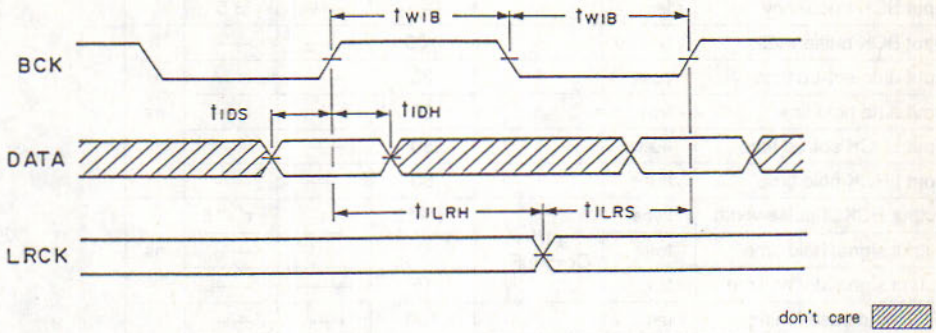
(V_{DD}=5V ± 10%, Vss=0V, Topr=–20 to 75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applied pin
Input voltage (1)	"H" level	V_{IH}		0.76V_{DD}			V	*1, *2, *3
	"L" level	V_{IL}				0.24V_{DD}		
Input voltage (2)	"H" level	V_{IH}	Input mode	2.0			V	*7
	"L" level	V_{IL}	Input mode			0.8		
Output voltage (1)	"H" level	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5			V	*5
	"L" level	V_{OL}	I_{OL}=2mA			0.4		
Output voltage (2)	"H" level	V_{OH}	V_{DD}=5.0V I_{OH}=–1mA		4.5		V	*6
	"L" level	V_{OL}	V_{DD}=5.0V I_{OL}=1mA		0.4			
Output voltage (3)	"H" level	V_{OH}	Output mode I_{OH}=–2mA	2.4			V	*7
	"L" level	V_{OL}	Output mode I_{OL}=1mA			0.4		
Output voltage (4)	"H" level	V_{OH}	I_{OH}=–2mA	2.4			V	*8
	"L" level	V_{OL}	I_{OL}=1mA			0.4		
Output voltage (5)	"H" level	V_{OH}	I_{OH}=–4mA	2.4			V	*9
	"L" level	V_{OL}	I_{OL}=2mA			0.4		
Input leak current (1)		I_{LI}	V_I=V_{DD}/0V			±5	μA	*1, *3
Input leak current (2)		I_{LI}	V_I=V_{DD}/0V			±10	μA	*2
Input leak current (3)		I_{LI}	V_I=V_{DD}/0V			±20	μA	*4
Input leak current (4)		I_{LI}	Input mode V_I=V_{DD}/0V			±10	μA	*7
Hysteresis voltage		V_H			1		V	*5
Pull-up resistance value		R_{IH}		7.5	15	30	kΩ	*2

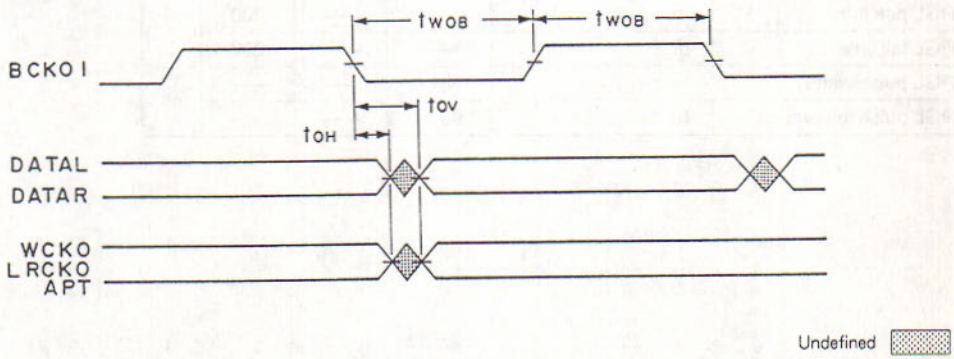
*1 DATA, BCK, LRCK, TEST, PRGD, PRGL
*2 8/4, 18/16, OFST, DPOL, DSP
*3 INIT, PRGCK, MUTE
*4 XIN
*5 BCKO1, DATA L, DATA R, WCKO, LRCKO, APT, SCK
*6 BCKO2
*7 I/O1 to I/O4
*8 WE, A0 to A8
*9 CAS, RAS

AC Characteristics

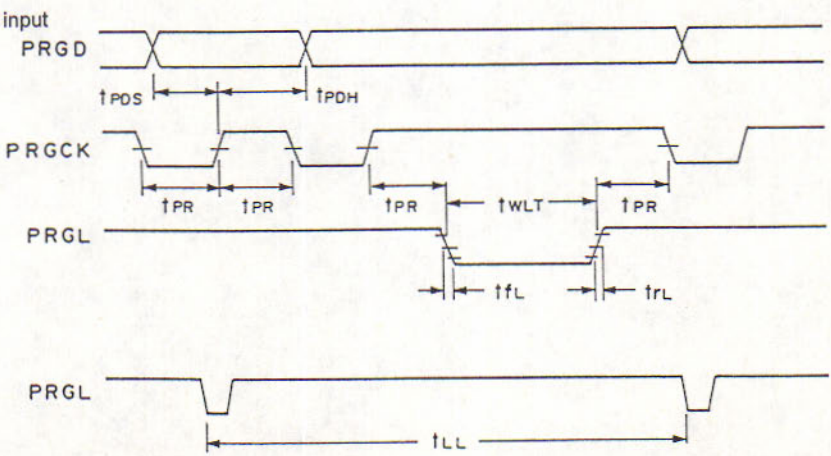
DATA input



Output



PRG input

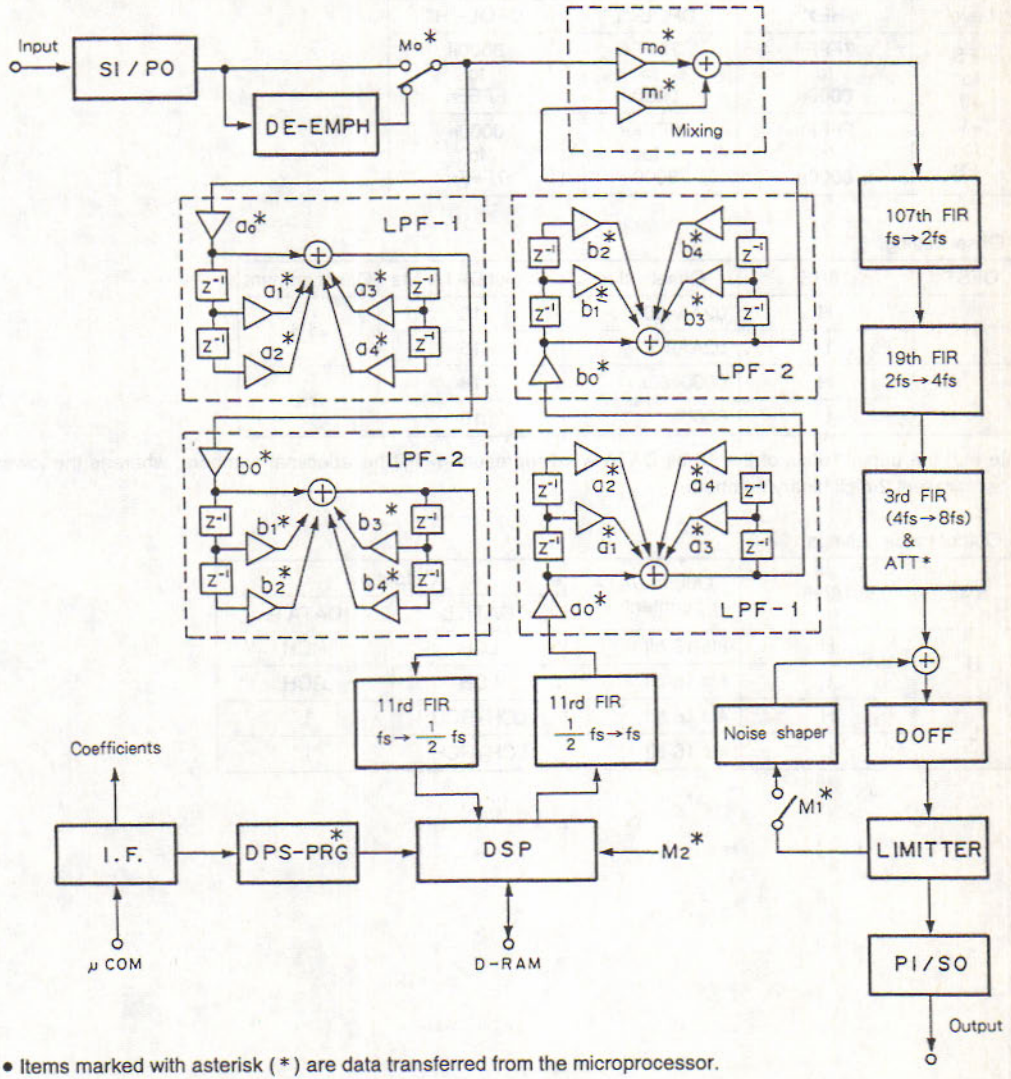


AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency	f_{XT}	f_{XT}=384fs	10	—	20	MHz
Input BCK frequency	f_{BCK}		—	—	3.5	
Input BCK pulse width	t_{WIB}		100	—	—	ns
Input data set-up time	t_{IDS}		20	—	—	
Input data hold time	t_{IDH}		20	—	—	
Input LRCK set-up time	t_{ILRS}		50	—	—	
Input LRCK hold time	t_{ILRH}		50	—	—	
Output BCKOI pulse width	t_{WOB}	τ =1/f_{XT} C_L=50pF	τ –15	τ	τ +15	ns
Output signal hold time	t_{OH}		0		—	
Output signal define time	t_{OV}		15	—	—	
PRG input base timing	t_{PR}		100	—	—	ns
PRGD set-up time	t_{PDS}		100	—	—	
PRGD hold time	t_{PDH}		100	—	—	
PRGL rise time	t_{rL}		—	—	200	
PRGL fall time	t_{fL}		—	—	200	
PRGL pulse width	t_{WLT}	τ =1/f_{XT}	4 τ	—	—	ns
PRGL pulse interval	t_{LL}		96 τ	—	—	

Description of Functions

Signal Flow



- Items marked with asterisk (*) are data transferred from the microprocessor.
  - DPS-PRG: DPS program
  - LPF-1 a_0, a_1, a_2, a_3, a_4, LPF-2 b_0, b_1, b_2, b_3, b_4: IIR filter coefficients
  - m_0, m_1: Mixing coefficients
  - ATT: Attenuator value
  - M_0, M_1, M_2: MODE (de-emphasis, noise shaping, DRAM select)
- At power on, all values are undefined.
- Z^{-1}: 1 sampling cycle delay

I/O Mode by Pin Settings

i) Input polarity setting (㊳DPOL)

Input DATA		Internally received DATA	
Level	HEX	DPOL="L"	DPOL="H"
+FS to +0	7FFFH to 0000H	7FFFH to 0000H	8000H to FFFFH
−1 to −FS	FFFFH to 8000H	FFFFH to 8000H	0000H to 7FFFH

ii) Offset settings

OFST	18/16	Offset value	Output DATA bits	Offset amount
H	H	02AAH00B	18	+1%
	L	02AAH	16	
L	H	0000H00B	18	0%
	L	0000H	16	

Note that the upper 16bits of the 18-bit DATA word represent 4-digit hexadecimal numbers; whereas the lower 2bits represent 2-digit binary numbers.

iii) Output mode settings

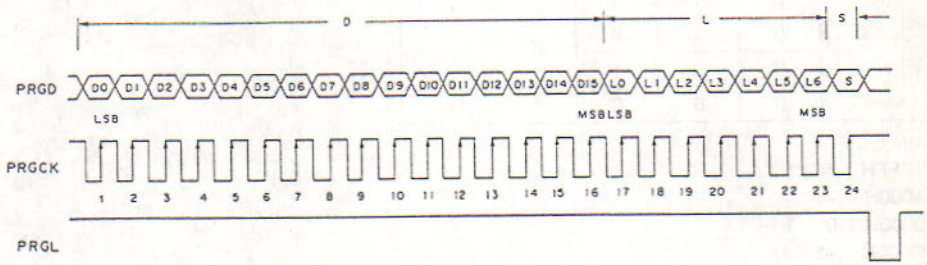
8/4	18/16	Output DATA contents	Output pin	
			DATA L	DATA R
H	H	8fs 18-bit	LCH	RCH
	L	8fs 16-bit	LCH	RCH
L	H	4fs 18-bit	LCH+RCH	"L"
	L	4fs 16-bit	LCH+RCH	"L"

Microcomputer Interface

Suppose that the microprocessor sends input to the pins shown in the figure below. The CXD1355AQ's internal DSP program, IIR filter coefficient, MIX coefficient and attenuation values can be re-written partially or totally depending on which of the various operating modes is selected.

- PRGDT ····· 24-bit length serial data transferred in one cycle
- PRGCK ····· The serial clock. When triggered by the rising edge of this signal, the serial data is transferred to the internal shift register.
- PRGL····· The entire contents of the 24-bit length serial data in the shift register is latched by the gate pass (active low level). At the same time, the rising edge of this signal initiates an internal request for processing.
- DSP····· When set "L", the DSP program and K-RAM data transfer function is disabled. MIX coefficient is fixed at m0=1, m1=0.

This transfer format (next item) timing are shown in the figure below.



S (1-bit) : When set "L", transfers DSP information; when "H", transfers non-DSP information.
L (7-bit) : Identification label for transfer data or transfer address information.
D (16-bit) : Transfer data; not used in MODE transfer operations.

L and D are in LSB first format
PRGD is triggered by the rising edge signal of PRGCK. The falling edge of PRGL latches the internal register.

Description of Modes

1) DATA RAM address
   External DRAM"s relative address

2) DSP coefficient instructions
   DSP program and coefficient
   The multiplication coefficient K (8-bit) of the DSP portion is equal to 7FH ≒ ×1, 80H = × (–1).

3) Filter coefficients

IIR filter coefficients and MIX coefficients.

When DSP mode is set "L", the following fixed values apply: m0 = × 1 (4000H), m1 = × 0 (0000H). Data may be set within the range $-2 \leqq$ DATA < 2.

Add					
A4	A3	A2	A1	A0	D15 to D0
1	1	x	x	x	m1
	0				m0
0	1	1	x	x	b4
		0	1	1	b3
		0	1	0	b2
		0	0	1	b1
		0	0	0	b0
	0	1	x	x	a4
		0	1	1	a3
		0	1	0	a2
		0	0	1	a1
		0	0	0	a0

DATA range

7FFFH : ≒ +2
4000H : +1
0000H : 0
C000H : –1
8000H : –2

4) ATT

ATT is the attenuation value. ATT data is made up of 16-bit. Bits D0 and D15 are ignored and processed as "0" data. Any data greater than 4000H is set to 4000H.

ATT setting value

D15 to D0	Setting value	
4000	4000	×1
|	|	|
0003	0002	|
0002	0002	|
0001	0000	|
0000H	0000H	×0

5) MODE

M0 : De-emphasis select. "H": ON, "L": OFF.

M1 : Noise shaping setting. "H": normal noise shaping ON.
"L": when ATT = x 1 (4000H), noise shaping is OFF.

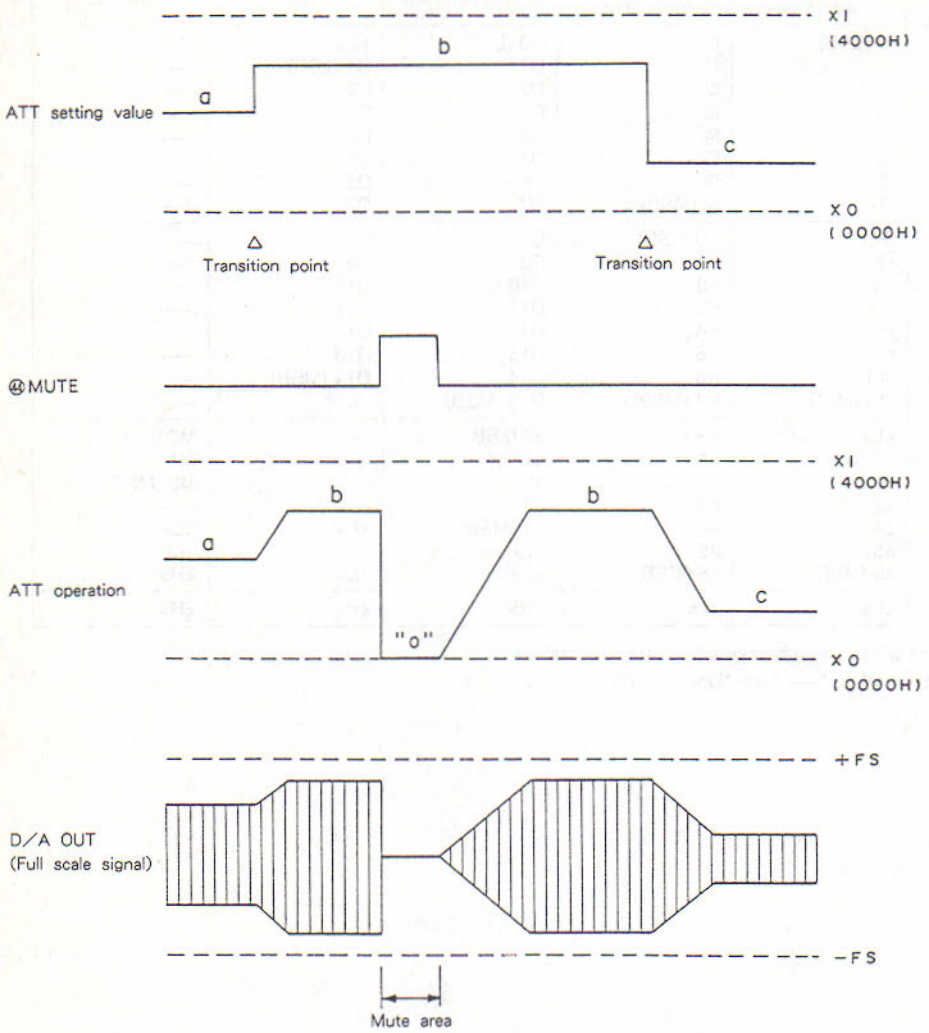
M2: External DRAM capacity select.
"H": 1M (256k x 4-bit) DRAM; "L": 256k (64k x 4-bit) DRAM. (Use page-mode DRAMs.)

Transfer Format

	DATA RAM address	DSP coefficient instruction	Filter coefficient	ATT	MODE
D0	r0 (LSB)	I0 (LSB)	D0 (LSB)	<L>	——
D1	r1	I1	D1	D1 (LSB)	——
D2	r2	I2	D2	D2	——
D3	r3	I3	D3	D3	——
D4	r4	I4	D4	D4	——
D5	r5	I5	D5	D5	——
D6	r6	I6	D6	D6	——
D7	r7	I7 (MSB)	D7	D7	——
D8	r8	K0 (LSB)	D8	D8	——
D9	r9	K1	D9	D9	——
D10	r10	K2	D10	D10	——
D11	r11	K3	D11	D11	——
D12	r12	K4	D12	D12	——
D13	r13	K5	D13	D13	——
D14	r14	K6	D14	D14 (MSB)	——
D15	r15 (MSB)	K7 (MSB)	D15 (MSB)	<L>	——
L0	<L>	<H>	a0 (LSB)	——	M0 (LSB)
L1	a1 (LSB)	a1 (LSB)	a1	——	M1
L2	a2	a2	a2	——	M2 (MSB)
L3	a3	a3	a3	——	——
L4	a4	a4	a4 (MSB)	<L>	<L>
L5	a5	a5	<L>	<H>	<L>
L6	a6 (MSB)	a6 (MSB)	<L>	<L>	<H>
S	<L>	<L>	<H>	<H>	<H>

* Items within angle brackets "< >" are fixed values.
* Items marked "——" are "Don't care."

ATT Operation

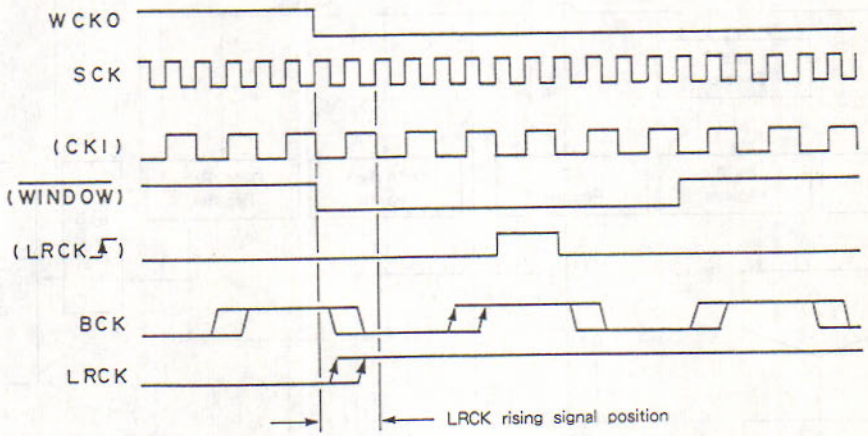


The time period during the ATT operation"s rising and falling signal is equal to 23.22mS/FS. (fs=44.1kHz) FS: Full scale.
Continuous input of Input DATA occurs even during mute operations.

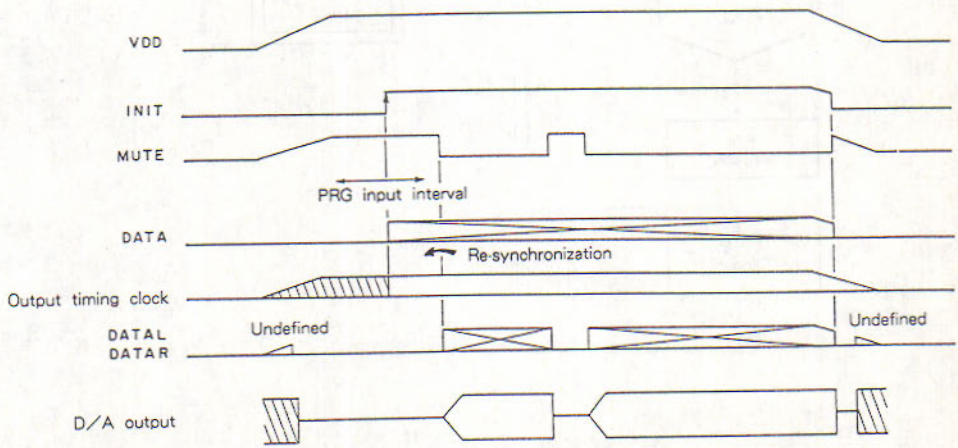
Synchronization

i) INIT re-synchronization
Re-synchronization is triggered by the rising edge timing of INIT. After the synchronization circuit clears out the previous synchronization timing, synchronization is reset. By this means the differential signal of the rising LRCK signal (LRCK ⎍) is placed in the center of the synchronization window (WINDOW).

ii) LRCK rising signal position
The synchronization circuit is controlled by clock signal CK1 (fXT/2). Depending on external IC conditions, LRCK is triggered by clock SCK (fXT). During synchronization, the rising edge of LRCK is valid between the two points shown in the diagram below.

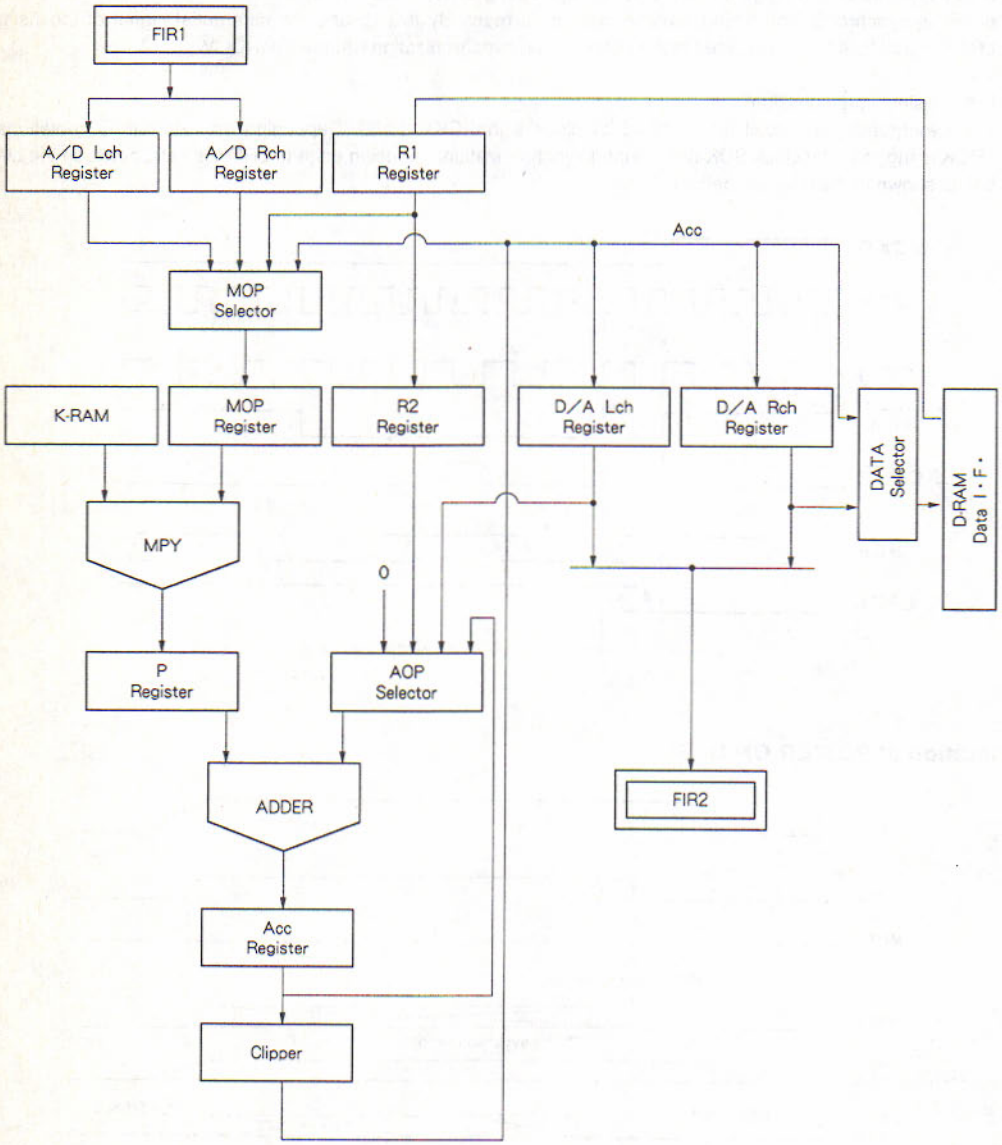


Operation at POWER ON/OFF



Description of DSP

★ DSP Block Diagram



Explanation of DSP Block Diagram

FIR 1	1/2fs down-sampling performed by 11th FIR filter.
FIR 2	Original fs up-sampled signal undergoes DSP signal processing to 1/2fs by 11th FIR filter.
A/D Lch Register	Register (ADL) stores L channel 16-bit data input from FIR1.
A/D Rch Register	Register (ADR) stores R channel 16-bit data input from FIR1.
D/A Lch Register	Register (DAL) stores L channel 16-bit data output from FIR2. Also used as addition 1st register.
D/A Rch Register	Register (DAR) stores R channel 16-bit data output from FIR2. Also used as a temporary register fordata output during I/O command operations.
R1 Register	Register (R1) stores the received 16-bit value during data I/O operations.
R2 Register	Register (R2) stores the R1 register data 16-bit by register transfer command.
K-RAM	RAM (K) stores 2's complement format, 8-bit multiplication coefficients.
MOP Register	Register (MOP) stores the 16-bit data instruction selected from the multiplication instruction command, ADL, ADR, R1, Acc (16).
MPY	Executes each operation in sequence: MOP (16) × K (8) → P (20).
P Register	Register (P) for storing 16-bit x 8-bit length results of multiplication 20-bit.
AOP Selector	Selects DAL, R2, Acc or zero from the additional instructions. Data is converted to 22-bit length format. (AOP)
ADDER	Executes each operation in sequence: AOP (22) + P (20) → Acc (22).
Acc Register	Register for storing 22-bit × 20-bit length results of addition 22-bit (Acc (22), Acc(16)).
Clipper	The 22-bit length addition result in Acc (22) is used as is by the subsequent addition command. In other operations, when there are 16-bit length operands and an overflow occurs, clipper processing is performed to make 16-bit length data which is then output to Acc (16).

Explanation of Instruction

A single instruction word is 8-bit length can handle parallel execution the following five instructions.

1. Multiplication instruction
   Depending on the setting of the multiplicand select bits (I0, I1), either R1, ADL, ADR or ACC * is used as the 16-bit multiplicand. This is multiple by the multiplication coefficient K and the product is latched to P. The resultant product P is used in the next addition instruction step. Equations such as (–1) x (–1) → + 1 will be calculated correctly.
   * Note that Acc contains 16-bit data resulting from overflow processing.

I1	I0	MPY
0	0	ADR × K
0	1	Acc × K
1	0	ADL × K
1	1	R1 × K

2. Addition instruction
   Depending on the setting of the augend select bits (I4, I5), either Acc (22), R2, DAL or zero value is used as the augend. The multiplication result P from the previous step is added to this and the addition result is latched to Acc (22).

I5	I4	Adder
0	0	0+P
0	1	R2+P
1	0	Acc+P
1	1	DAL+P

3. Data I/O instruction
   During a read cycle (I7 = "H"), input data is latched to R1. During a write cycle (I7 = "L"), either Acc or DAR are selected, depending on the setting of I2 and I3, and the data is output. During write cycles, data in R1 does not change.

I7	I3	I2	DRAM	DATA
0	0	0	WRITE	DAR → DRAM
0	0	1		Acc → DRAM
0	1	X		Acc → DRAM
1	X	X	READ	DRAM → R1

4. Acc transfer instruction
   Depending on the setting of the Acc transfer bits (I2, I3), Acc can transfer to either DAL or DAR.

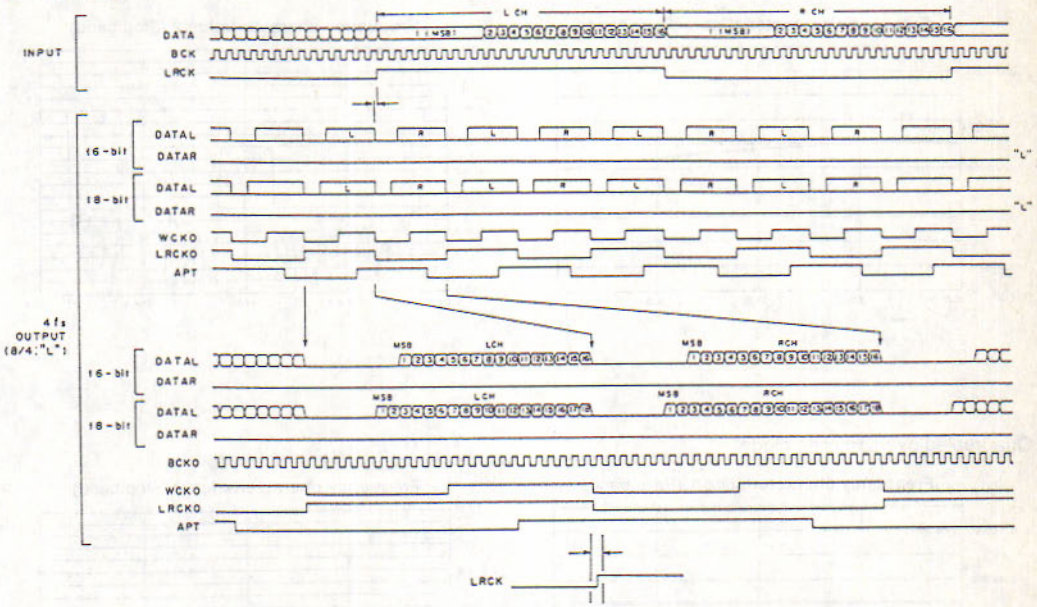
I3	I2	Acc transfer
0	X	——
1	0	Acc → DAL
1	1	Acc → DAR

5. R1 transfer instruction
   Depending on the setting of the register transfer bit (I6), R1 data transfer to R2 is selected. I6 = "H": R2 value remains unchanged.

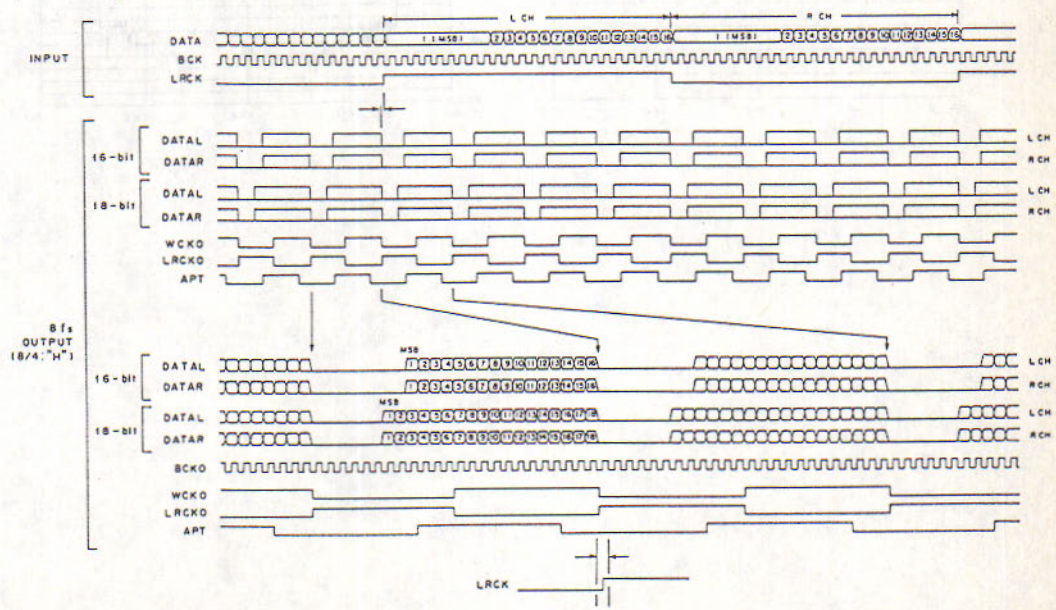
I6	R1 transfer
0	R1 → R2
1	——

I/O Timing

i) 4fs timing



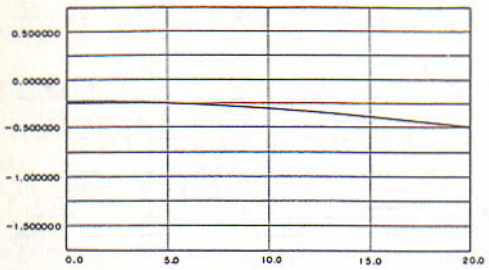
ii) 8fs timing



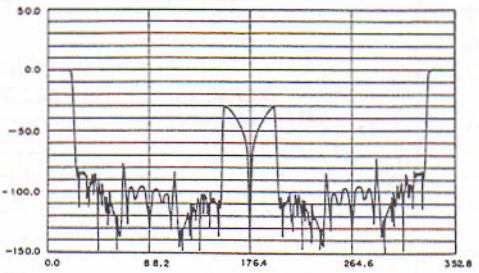
Filter Characteristics

Octupled oversampling mode

Frequency characteristics 1 (Pass band)

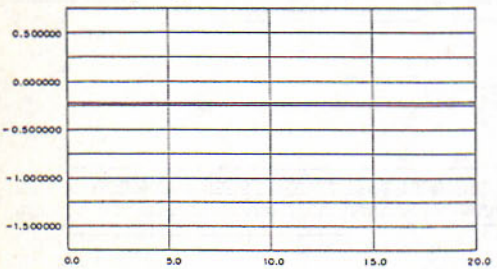


Frequency characteristics 2 (Stop band)

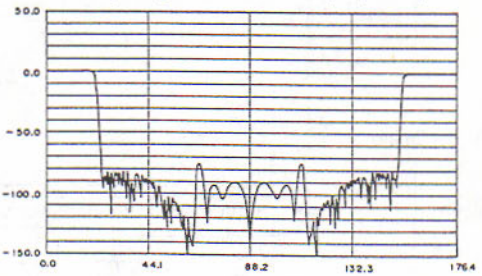


Quadrupled oversampling mode

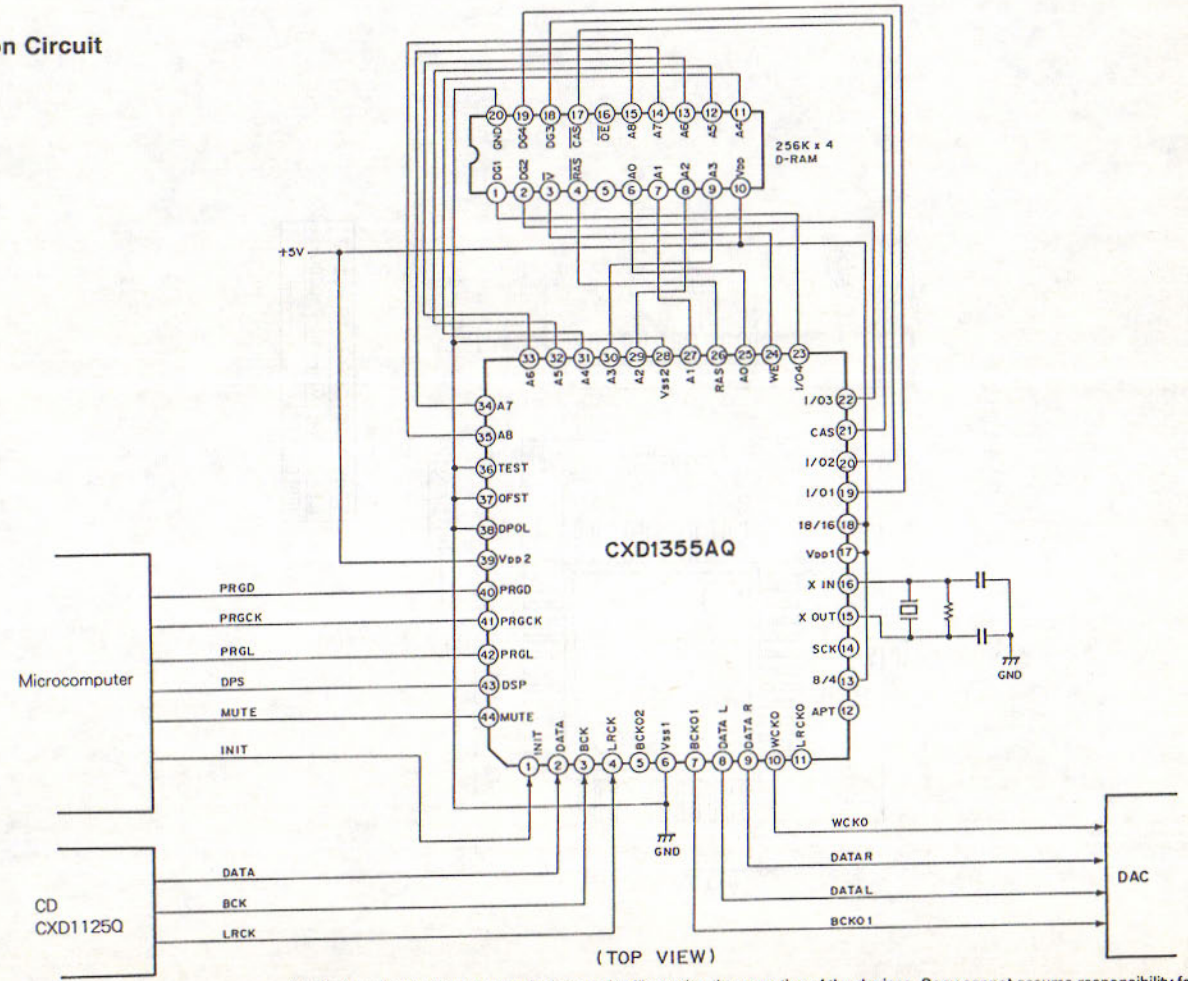
Frequency characteristics 1 (Pass band)



Frequency characteristics 2 (Stop band)



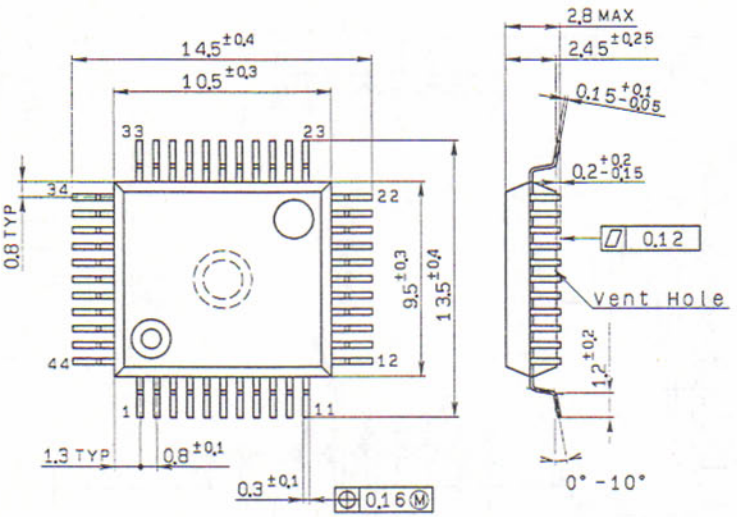
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

44Pin QFP (Plastic)



SONY NAME	QFP-44P-L102
EIAJ NAME	XQFP044-P-0000-BU
JEDEC CODE	———

SONY

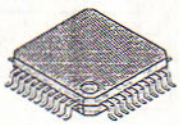
CXD2701Q

Digital Signal Processing LSI for Audio

Description

The CXD2701Q digital signal processing LSI incorporates both reverb and equalizer functions into a single IC capable of handling 2-channel digital audio signals.

44 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Features

- Uses external DRAM for delay signal processing. Sound field processing features such as delay, echo, and reverb are software programmable.
- Frequency response of the parametric equalizer can be dynamically changed by using the program setting to vary the coefficient value.

Functions

- 2 channels
- 24-bit word-length data processing
- Programmable sound field processing
  Pre-sound field processing using down-sampling (fs→fs/2),
  Post-processing with up-sampling (fs/2→fs)
- Uses external DRAM, either 64K×4-bit or 256K×4-bit for delay control.
- Delay amount for L and R channels can be set to a maximum of 64K delay samples
- Built-in 32-bit equalizer register
- Digital de-emphasis function (32K, 44.1K, 48K)
- Input/Output format
  Input : Two's complement MSB first, LSB first (24-bit or 16-bit)
  Output : Two's complement MSB first, LSB first (24-bit, 20-bit, 18-bit or 16-bit)

Absolute Maximum Ratings (Ta=25°C, Vss=0V)

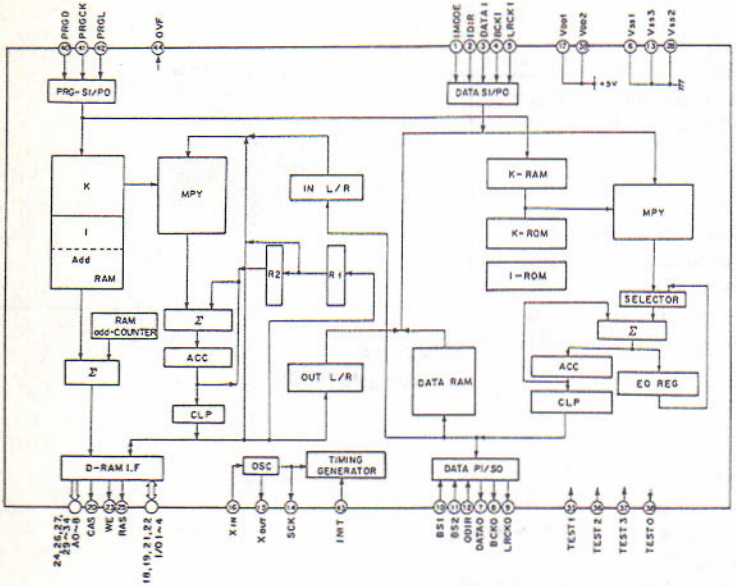
• Supply voltage	V_{DD}	Vss–0.3 to +7.0	V
• Input voltage	V_I	Vss–0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Output current	Io	–10 to +10	mA

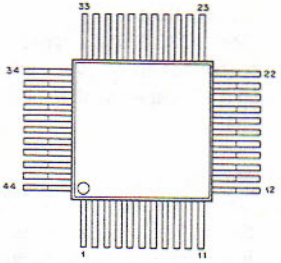
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0V Typ.)	V
• Operating temperature	Topr	–20 to +75	°C
• OSC frequency	fxt	15 to 25	MHz

E90Y07 – ST

Block Diagram and Pin Configuration (Top View)





Pin Description

Pin No.	Symbol	I/O	Description
1	IMODE	I	Input data format select pin. Data format toggled by "High" and "Low" position.
2	IDIR	I	Input data format select pin. When set "High", MSB first; when set "Low", LSB first.
3	DATAI	I	Single sampling, 2-channel serial input pin. Data is in two's complement format.
4	BCKI	I	Serial bit clock input for serial input data.
5	LRCKI	I	Serial input/output sampling frequency clock input pin. When set "High", L-channel data is transferred; when set "Low", R-channel data.
6	Vss1	——	Ground pin
7	DATAO	O	Serial data output pin. Two's complement data format.
8	BCKO	O	Bit clock output pin. 64 slot.
9	LRCKO	O	Output for sampling frequency clock's serial data.
10	BS1	I	Output data, bit select pin. BS2=H, BS1=H 24bit BS2=H, BS1=L 20bit BS2=L, BS1=H 18bit BS2=L, BS1=L 16bit
11	BS2	I	
12	ODIR	I	Output data format select pin. When set "High", MSB first, when set "Low", LSB first.

Pin No.	Symbol	I/O	Description
13	Vss3	——	Ground pin.
14	SCK	O	System clock output pin. fsck=fxt=512fs
15	XOUT	O	Crystal oscillator output pin.
16	XIN	I	Crystal oscillator input pin. fxt=512fs
17	$V_{DD}1$	——	+5V power supply pin
18	I/O4	I/O	External DRAM data input/output I/O4.
19	I/O3	I/O	External DRAM data input/output I/O3.
20	CAS	O	Column address strobe output for external DRAM.
21	I/O2	I/O	External DRAM data input/output I/O2.
22	I/O1	I/O	External DRAM data input/output I/O1.
23	WE	O	External DRAM write-enable output pin. Effective at "Low".
24	A0	O	External DRAM address output A0.
25	RAS	O	External DRAM row-address strobe output pin.
26	A1	O	External DRAM address output A1.
27	A2	O	External DRAM address output A2.
28	Vss2	——	Ground pin.
29	A3	O	External DRAM address output A3.
30	A4	O	External DRAM address output A4.
31	A5	O	External DRAM address output A5.
32	A6	O	External DRAM address output A6.
33	A7	O	External DRAM address output A7.
34	A8	O	External DRAM address output A8.
35	TEST1	I	Test pin. Normally set to Ground.
36	TEST2	I	Test pin. Normally set to Ground.
37	TEST3	I	Test pin. Normally set to Ground.
38	TEST0	O	Test pin.
39	$V_{DD}2$	——	+5V power supply pin.
40	PRGD	I	Receives serial input sent from microprocessor including instructions, coefficients, and control data.
41	PRGCK	I	Serial clock input for PRGD signal. Data are accepted at rising.
42	PRGL	I	Latch input pin used to internally latch serial data sent from microprocessor. Active when set "Low".
43	INIT	I	Initialization pin. Effective at "Low". It is re-synchronized at rising.
44	OVF	O	Overflow flag output for 5-bit; DSP, L-channel MIX, R-channel MIX, L-channel EQ, and R-channel EQ.

Electrical Characteristics

Input Capacitance

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin *1	C_{IN}			3	5	pF
Input pin *2	C_{IN}	Input mode		4	6	pF

*1. All except Input/Output pins
*2. Input/Output pins

DC Characteristics

(V_{DD}=5V ± 10%, V_{SS}=0V, T_{OP}=–20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pin
Input voltage (1)	H level	V_{IH}		0.76V_{DD}			V	*1, *2
	L level	V_{IL}				0.24V_{DD}		
Input voltage (2)	H level	V_{IH}	Input mode	2.4			V	*5
	L level	V_{IL}	Input mode			0.8		
Output voltage (1)	H level	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5			V	*4
	L level	V_{OL}	I_{OL}=2mA			0.4		
Output voltage (2)	H level	V_{OH}	Output mode I_{OH}=–2mA	2.4			V	*5
	L level	V_{OL}	Output mode I_{OL}=1mA			0.4		
Output voltage (3)	H level	V_{OH}	I_{OH}=–2mA	2.4			V	*6
	L level	V_{OL}	I_{OL}=1mA			0.4		
Output voltage (4)	H level	V_{OH}	I_{OH}=–4mA	2.4			V	*7
	L level	V_{OL}	I_{OL}=2mA			0.4		
Input leak current (1)		I_{LI}	V_I=V_{DD}/0V			±5	μA	*1, *2
Input leak current (2)		I_{LI}	V_I=V_{DD}/0V			±40	μA	*3
Input leak current (3)		I_{LI}	Input mode V_I=V_{DD}/0V			±10	μA	*5
Hysteresis voltage		V_H			1		V	*2

*1. DATAI, BCKI, LRCKI, PRGD, PRGL, IMODE, IDIR, BS1, BS2, ODIR
*2. INIT, PRGCK
*3. XIN
*4. BCKO, DATAO, LRCKO, SCK, OVF
*5. I/O1 to I/O4
*6. WE, A0 to A8
*7. CAS, RAS

AC Characteristics

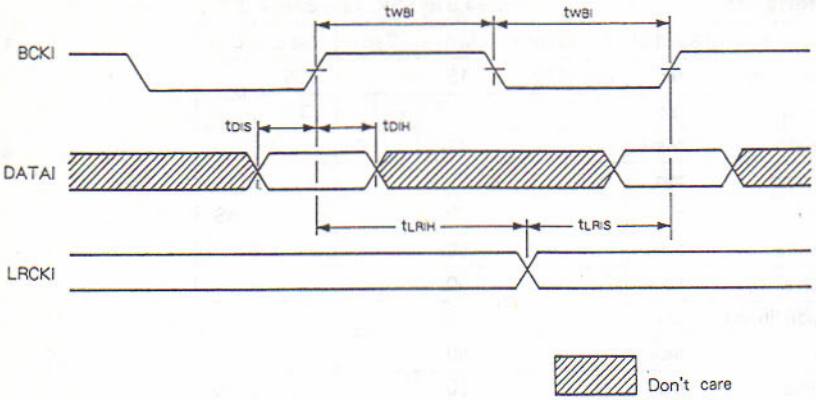
AC Characteristics I

(V_{DD}=4.5 to 5.5V, Ta=–20 to +75°C)

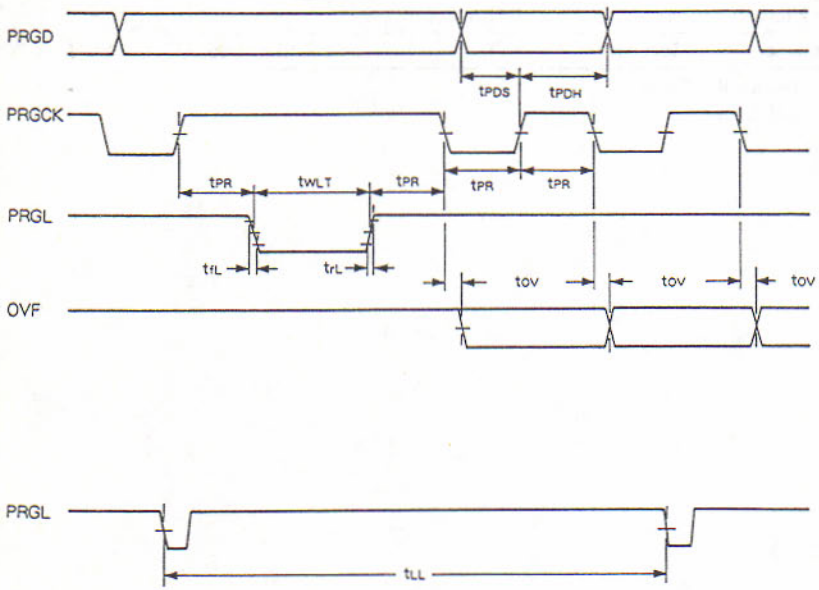
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency	f_{XT}	f_{XT}=512fs	15		25	MHz
BCKI frequency	f_{BCK}				3.5	
BCKI pulse width	t_{WBI}		100			nS
DATAI setup time	t_{DIS}		20			
DATAI hold time	t_{DIH}		20			
LRCKI setup time	t_{LRIS}		50			
LRCKI hold time	t_{LRIH}		50			
PRG input base timing	t_{PR}		100			nS
PRGD setup time	t_{PDS}		50			
PRGD hold time	t_{PDH}		50			
PRGL rise time	t_{rL}				200	
PRGL fall time	t_{fL}				200	
PRGL pulse width	t_{WLT}	$\tau = 1/f_{XT}$	8 τ			
PRGL pulse interval	t_{LL}		512 τ			
OVF defined time	tov				40	nS

* Timing specified level: 0.5V_{DD}
t_{fL}=0.1V_{DD}, trL=0.9V_{DD}

DATA Input



PRG Input/Output



Timing specified level : 0.5V_{DD}
tfL = 0.1V_{DD}, trL = 0.9V_{DD}

AC Characteristics II

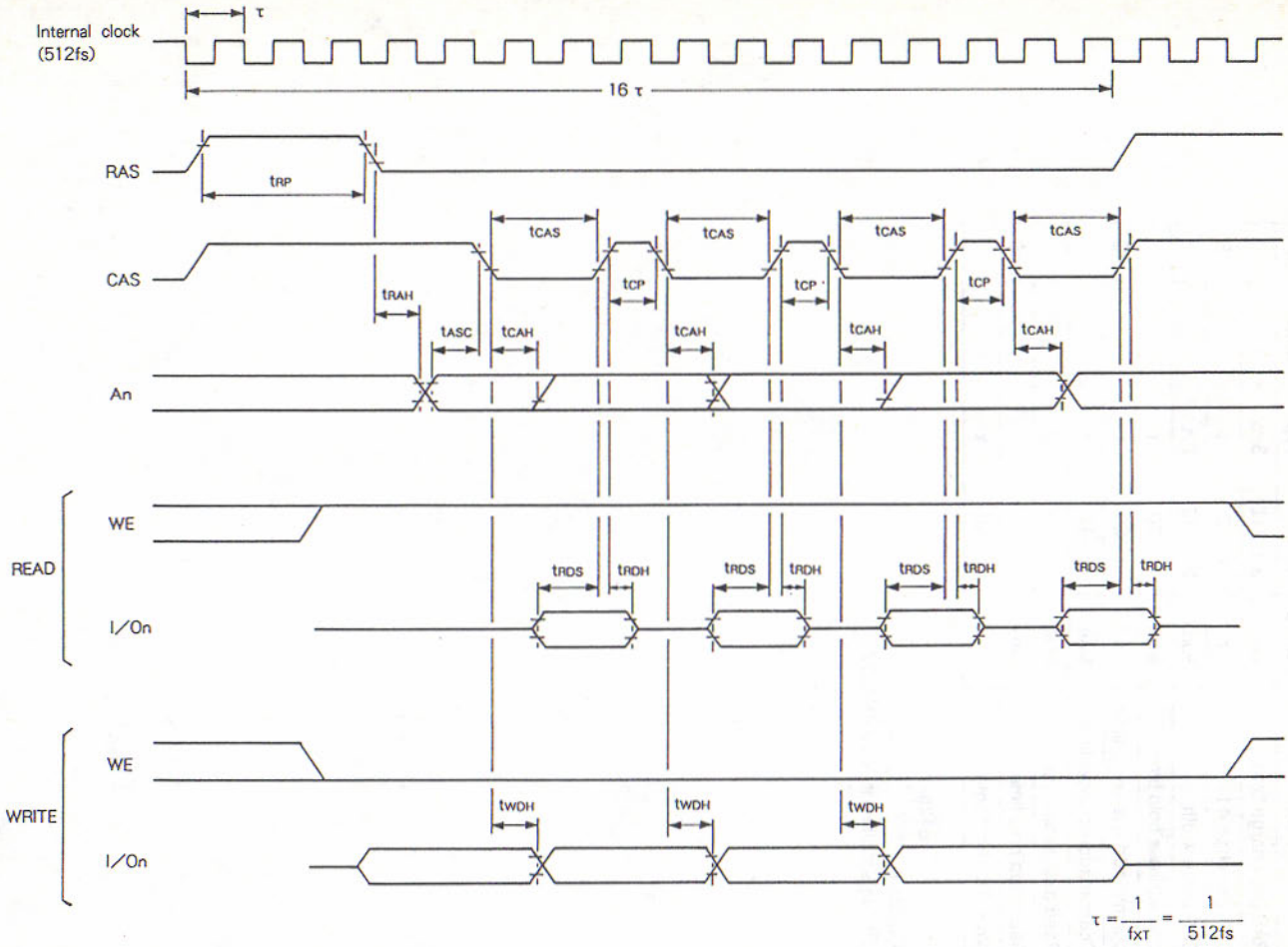
(V_{DD}=4.5 to 5.5V, Ta=–20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
RAS pre-charge time	t_{RP}	3 τ –12	3 τ		nS
CAS pre-charge time	t_{CP}	τ –12	τ		
CAS pulse width	t_{CAS}	2 τ –12	2 τ		
Low address hold time	t_{RAH}	τ –20	τ		nS
Column address setup time	t_{ASC}	τ –20	τ		
Column address hold time	t_{CAH}	τ –18	τ		
Read data setup time	t_{RDS}	20			nS
Read data hold time	t_{RDH}	5			
Write data hold time	t_{WDH}	τ –18	τ		

- $\tau = \frac{1}{f_{XT}} = \frac{1}{512fs}$
- C_L=30pF
- Timing specified level: 2.4V/0.8V

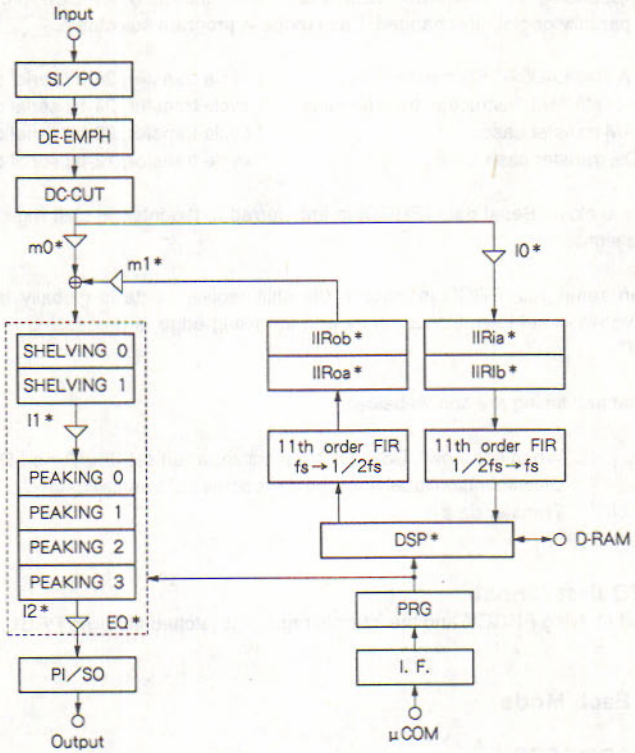
DRAM Access Timing

(High-speed page mode)



Description of Functions

Signal Flow Diagram



- * Asterisk items represent data transferred from the microprocessor.
  - EQ: Equalization coefficient
  - DSP: DSP program, coefficient
  - IIRoa, IIRob, IIRia, IIRib: IIR filter coefficients
  - m0, m1: mixing coefficient
  - I0, I1, I2: coefficients
- All above values for current charging times are undefined.

Microprocessor Interface

Control instructions from the microprocessor are carried out under the three assumptions list below (PRGD, PRGCK, PRGL). Depending on how these factors are setup internally for DSP program, IIR filter and MIX coefficients can be partially or globally changed. Each mode is program selectable.

- PRGD ····· DATA RAM ADDRESS transfer case — 1 cycle transfer, 24-bit serial data
  DSP coefficient, Instruction transfer case — 1 cycle transfer, 24-bit serial data
  K-RAM transfer case — 1 cycle transfer, 28-bit serial data
  MODE transfer case — 1 cycle transfer, 12-bit serial data

- PRGCK ····· A serial clock. Serial data (PRGD) is transferred to the internal shift register activated by the rising edge signal.

- PRGL ····· When serial data PRGD is input to the shift register, data is globally latched by the gate pulse (active when set low). Concurrently with the rising edge, a processing request is sent internally to the IC.

The transfer format and timing are shown below:

S (1-bit) : When set "Low", DSP transfers active; when set "High", non-DSP transfers.
L (7-bit/3-bit) : Discrimination label and transfer address of transfer data
D (16-bit/20-bit/8-bit) : Transfer data

L and D use LSB first format

PRGD is accepted at rising PRGCK and the internal register is latched at falling PRGL.

Explanation of Each Mode

1) DATA RAM, ADDRESS

External DRAM relative address

2) DSP coefficient INSTRUCTION

DSP program and coefficient.
DSP section multiplication coefficient K (8-bit) is equal to 7FH ≒ ×1, 80H= ×(–1).

Transfer Formats

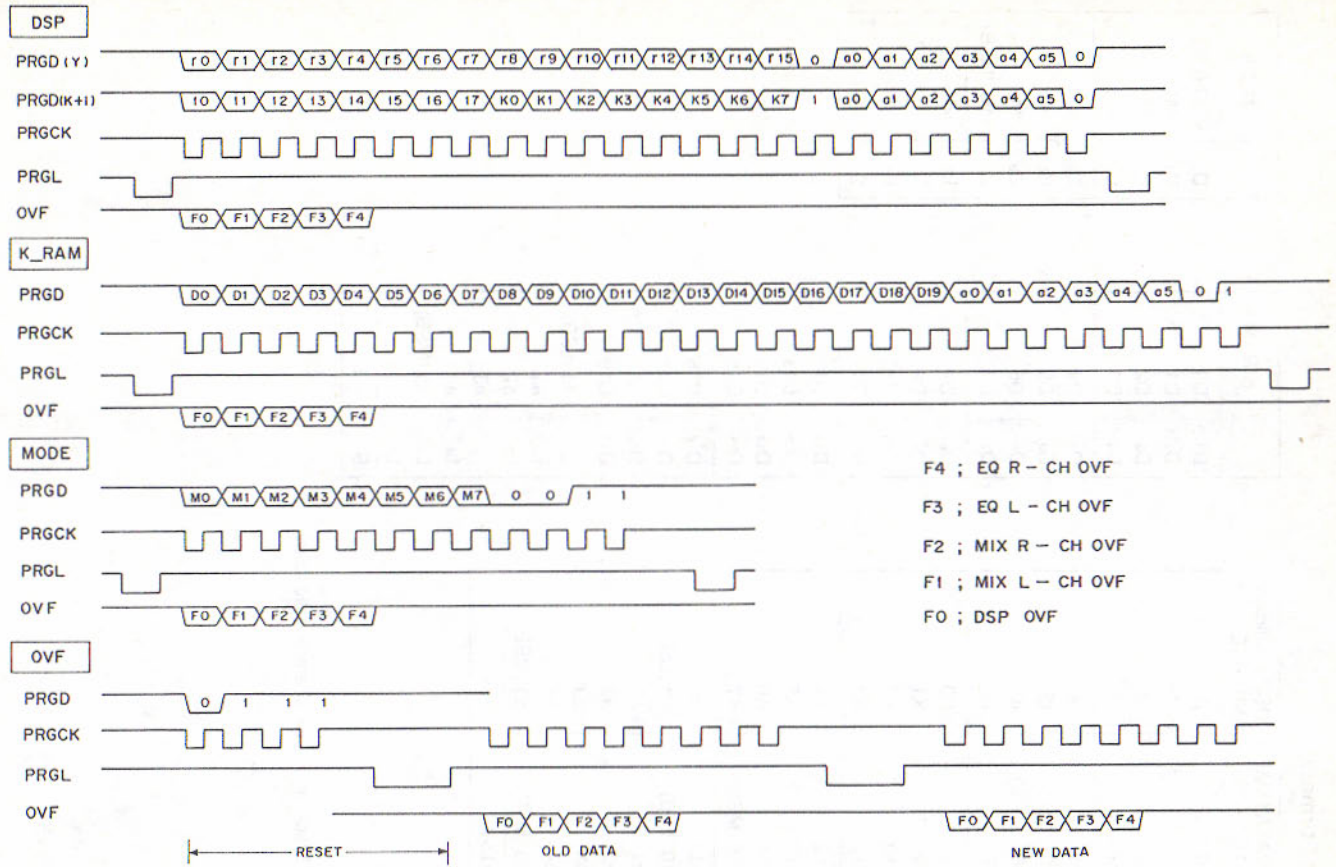
	DATA RAM ADDRESS	DSP coefficient INSTRUCTION
D_0	r0 (LSB)	I0
D_1	r1	I1
D_2	r2	I2
D_3	r3	I3
D_4	r4	I4
D_5	r5	I5
D_6	r6	I6
D_7	r7	I7
D_8	r8	K0
D_9	r9	K1
D_{10}	r10	K2
D_{11}	r11	K3
D_{12}	r12	K4
D_{13}	r13	K5
D_{14}	r14	K6
D_{15}	r15 (MSB)	K7
L_0	<L>	<H>
L_1	a0 (LSB)	a0 (LSB)
L_2	a1	a1
L_3	a2	a2
L_4	a3	a3
L_5	a4	a4
L_6	a5 (MSB)	a5 (MSB)
S	<L>	<L>

	K-RAM
D_0	D0
D_1	D1
D_2	D2
D_3	D3
D_4	D4
D_5	D5
D_6	D6
D_7	D7
D_8	D8
D_9	D9
D_{10}	D10
D_{11}	D11
D_{12}	D12
D_{13}	D13
D_{14}	D14
D_{15}	D15
D_{16}	D16
D_{17}	D17
D_{18}	D18
D_{19}	D19
L_0	a0 (LSB)
L_1	a1
L_2	a2
L_3	a3
L_4	a4
L_5	a5 (MSB)
L_6	<L>
S	<H>

	MODE
D_0	M0 (LSB)
D_1	M1
D_2	M2
D_3	M3
D_4	M4
D_5	M5
D_6	M6
D_7	M7 (MSB)
L_0	<L>
L_1	<L>
L_2	<H>
S	<H>

* Items in brackets < > are characteristic values

PRG Input/Output Timing



3) K-RAM

Parametric equalizer coefficients

a_5	a_4	a_3	a_2	a_1	a_0	DATA		
1	1	1	1	1	1	PG_{31}	R	PEAKING 3
					0	PG_{30}	L	
				0	1	B_3		
					0	F_3		
			0	1	1	PG_{21}	R	PEAKING 2
					0	PG_{20}	L	
				0	1	B_2		
					0	F_2		
		0	1	1	1	PG_{11}	R	PEAKING 1
					0	PG_{10}	L	
				0	1	B_1		
					0	F_1		
			0	1	1	PG_{01}	R	PEAKING 0
					0	PG_{00}	L	
				0	1	B_0		
					0	F_0		
	0	1	1	1	×	SG_{11}	R	SHELVING 1
				0	×	SG_{10}	L	
			0	1	×	PH_1		
				0	×	L_1		
		0	1	1	×	SG_{01}	R	SHELVING 0
				0	×	SG_{00}	L	
			0	1	×	PH_0		
				0	×	L_0		
0	1	1	1	1	1	b_4		IIR B
					0	b_3		
				0	1	b_2		
					0	b_1		
			0	×	×	b_0		
		0	1	1	1	a_4		IIR A
					0	a_3		
				0	1	a_2		
					0	a_1		
			0	×	×	a_0		
	0	1	1	×	×			
			0	1	1	I_{21}	R	LEVEL
					0	I_{20}	L	
				0	1	I_{11}	R	
					0	I_{10}	L	
		0	1	×	×	I_0		
			0	1	1	m_{11}	R	MIX
					0	m_{10}	L	
				0	1	m_{01}	R	
					0	m_{00}	L	

43W

4) MODE settings

M_7: EMPH1
M_6: EMPH0

M_7	M_6	Settings
1	1	48 kHz de-emphasis "ON"
	0	44.1 kHz de-emphasis "ON"
0	1	32 kHz de-emphasis "ON"
	0	De-emphasis "OFF"

M_5: DC-CUT

M_5	Settings
1	DC-CUT "ON"
0	DC-CUT "OFF"

M_4: DSP

M_4	Settings
1	DSP operation "ON"
0	DSP operation "OFF"

M_3: EQ

M_3	Settings
1	EQ operation "ON"
0	EQ operation "OFF"

M_2: TEST MODE

M_2	Settings
1	Test mode
0	Normal mode

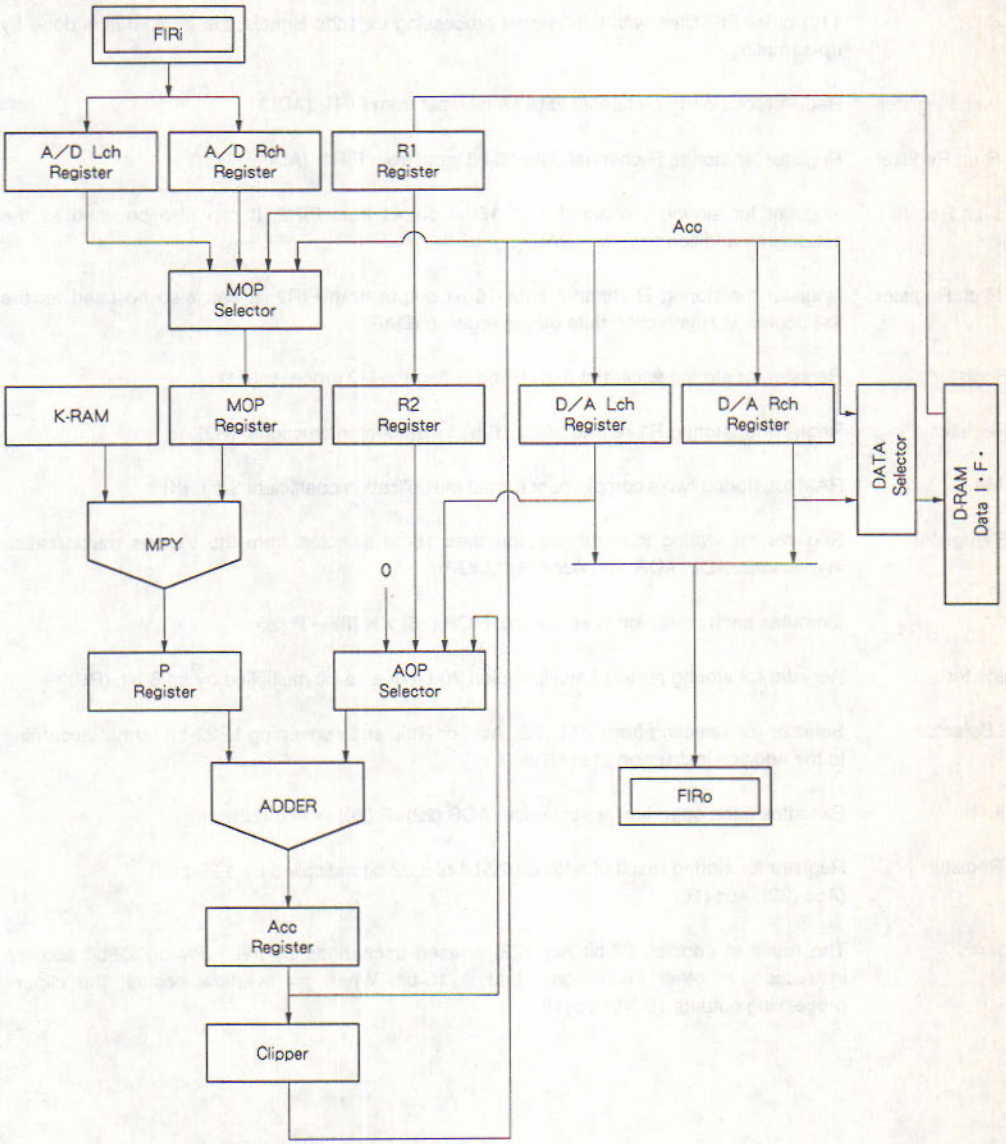
M_1: 1M/256

M_1	Settings
1	1M-bit external DRAM for DSP use
0	256K-bit external DRAM for DSP use

M_0: Not used.

DSP Explanation

DSP Section Block Diagram



DSP Block Diagram Explanation

FIR i	11th-order FIR filter, using 1/2fs down-sampling.
FIR o	11th-order FIR filter, with DSP signal processing by 1/2fs signals, the original fs is done by up-sampling.
A/D L-ch Register	Register for storing L-channel data 16-bit input from FIR1. (ADL)
A/D R-ch Register	Register for storing R-channel data 16-bit input from FIR1. (ADR)
D/A L-ch Register	Register for storing L-channel data 16-bit output from FIR2. It can also be used as the 1st-degree addition register. (DAL)
D/A R-ch Register	Register for storing R-channel data 16-bit output from FIR2. It can also be used as the 1st-degree I/O instruction data output register. (DAR)
R1 Register	Register for storing accepted data 16-bit during the I/O process. (R1)
R2 Register	Register for storing R1 register data 16-bit by transfer instructions. (R2)
K-RAM	RAM for storing two's complement format multiplication coefficient 8-bit. (K)
MOP Register	Register for storing the multiplication data 16-bit selected from the various multiplication instructions, ADL, ADR, R1, Acc (16). (MOP)
MPY	Executes each operation in sequence: MOP (16) ×K (8) → P (20).
P Register	Register for storing result of multiplication 20-bit of a 16-bit multiplied by an 8-bit. (P)
AOP Selector	Selector for selecting from DAL, R2, Acc, or Null, and converting to 22-bit format according to the addition instruction of each step.
ADDER	Executes each operation in sequence: AOP (22)+P (20) → Acc (22).
Acc Register	Register for storing result of addition 22-bit of a 22-bit multiplied by a 20-bit. (Acc (22), Acc (16))
Clipper	The result of addition 22-bit Acc (22) is used unchanged by the following 22-bit addition instruction. In other instructions, that is 16-bit. When an overflow occurs, the clipper processing outputs 16-bit Acc (16).

Explanation of Instruction

Among the 8-bit word-length instructions, the following five types of instructions are capable of parallel execution.

1. Multiplication instructions

Depending on the multiplicand select bits (I0,I1), one of the 16-bit data from R1, ADL, ADR, ACC * is selected as the multiplicand (16-bit). To this is multiplied the multiplication coefficient K. The result of multiplication is latched to P. The result P is used by the next addition instruction. This process also will correctly execute the problem $(-1)\times(-1) \rightarrow +1$.

* Acc is 16-bit data, overflow processing performed.

I1	I0	MPY
0	0	ADR×K
0	1	Acc×K
1	0	ADL×K
1	1	R1×K

2. Addition instructions

Depending on the augend select bits (I4, I5), one of the data from Acc (22), R2, DAL, or Null is selected as the augend. The multiplication result of pre step, P is added to this augend and the result latched to Acc (22).

I5	I4	Adder
0	0	0+P
0	1	R2+P
1	0	Acc+P
1	1	DAL+P

3. Data input/output instructions

During Read time (I7 is High), the input data is latched to R1. During Write time (I7 is Low), either Acc or DAR is selected (I2, I3) and this data is output. R1 remains unchanged during Write.

I7	I3	I2	DRAM	DATA
0	0	0	WRITE	DAR → DRAM
0	0	1		Acc → DRAM
0	1	X		Acc → DRAM
1	X	X	READ	DRAM → R1

4. Acc transfer instructions

Depending on Acc transfer bits (I2, I3), Acc can be transferred to either DAL or DAR.

I3	I2	Acc transfer
0	X	——
1	0	Acc → DAL
1	1	Acc → DAR

5. R1 transfer instructions

Depending on the register transfer bit (I6), R1 data can be transferred to R2. If I6 is High, R2's value remains unchanged.

I6	R1 transfer
0	R1 → R2
1	——

Cautions when using DRAMs

DRAM Address

The DRAM address generation section has a 16-bit binary counter incremented during 2/fs (program cycles). Absolute address (b_{15} to b_0) are generated.

The DRAM addresses (a_{15} to a_0) assume the value calculated by adding the absolute addresses (b_{15} to b_0) and the DSP programming relative addresses (r_{15} to r_0).

(a_{15} to a_0) = (b_{15} to b_0) + (r_{15} to r_0)

Carry-over is ignored.

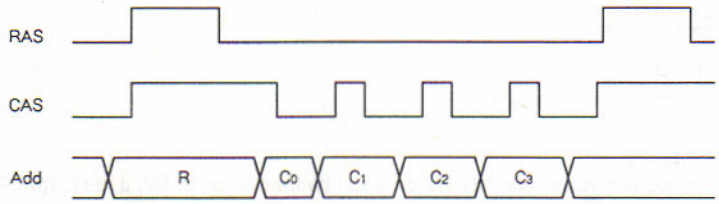
In the case of 256K DRAMs, in order for the upper 2 bits (a_{15} and a_{14}) not to be used among relative addressing, addresses r_{15} and r_{14} are made invalid.

<IM D-RAM>

Add \ Pin Name		A8	A7	A6	A5	A4	A3	A2	A1	A0
Row	R	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0
Column	C_0	a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	0	0
	C_1								0	1
	C_2								1	0
	C_3								1	1

<256K D-RAM>

Add \ Pin Name		A8	A7	A6	A5	A4	A3	A2	A1	A0
Row	R	—	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0
Column	C_0	—	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	0	0
	C_1								0	1
	C_2								1	0
	C_3								1	1



Fast page mode

DRAM Refresh

Normal DRAM refresh timings are as follows:

256K DRAMs: 4 msec/256 times

1M DRAMs: 8 msec/512 times

As the row address of the DRAM in DSP in DSP mode is incremented each program cycle 2/fs, the number (N) of refresh times during 2/fs is calculated as follows:

$$\frac{2}{fs} \times \frac{1}{N} \leqq \frac{4mS}{256} = \frac{8mS}{512}$$

$$N \geqq \frac{128}{fs}$$

fs=32kHz	fs=44.1kHz	fs=48kHz
N ≧ 4.0	N ≧ 2.9	N ≧ 2.7

In order that all low address refresh is completed within the defined time so that all low address delay periods are equal to N time accesses (leading), be sure to set relative address (r_{15} to r_0).

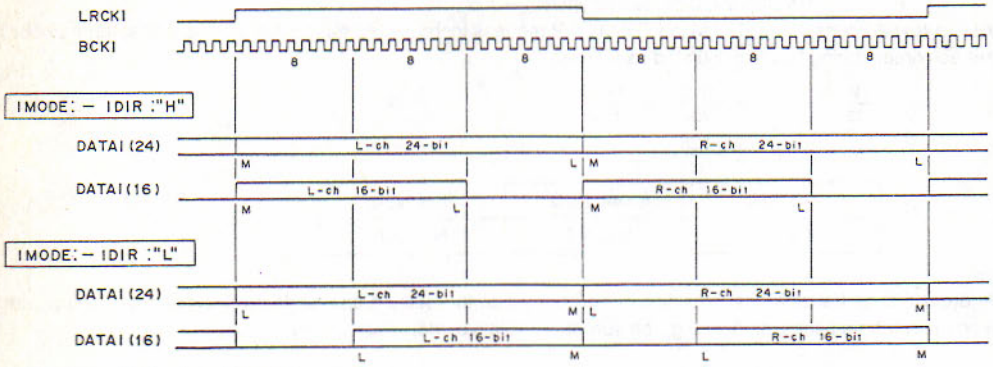
Example: When N=4 times, set following addresses:

<256K D-RAM>
- 0000H
- 0040H
- 0080H
- 00C0H

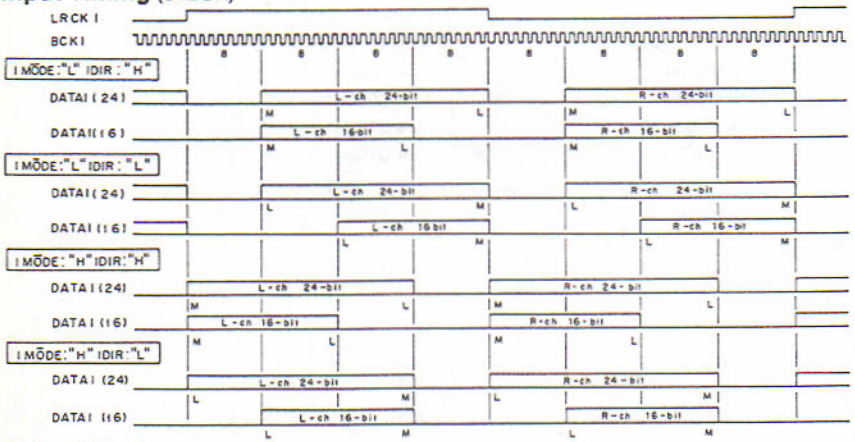
<1M D-RAM>
- 0000H
- 0080H
- 0100H
- 0180H

Input/Output Timing

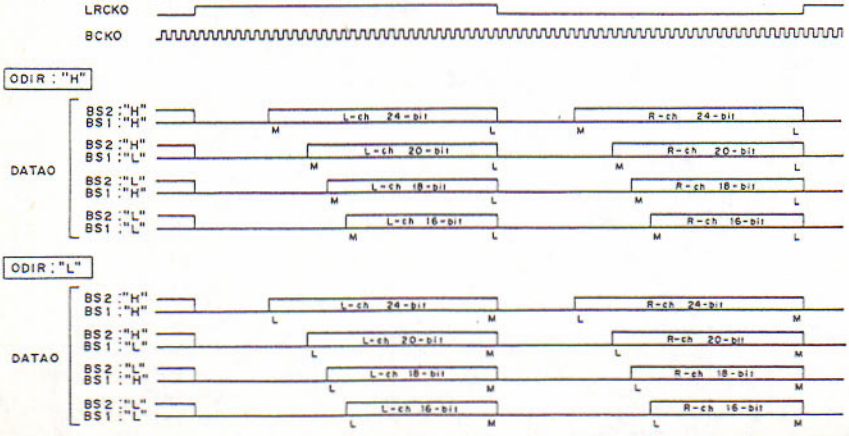
DATA Input Timing (48BCK)



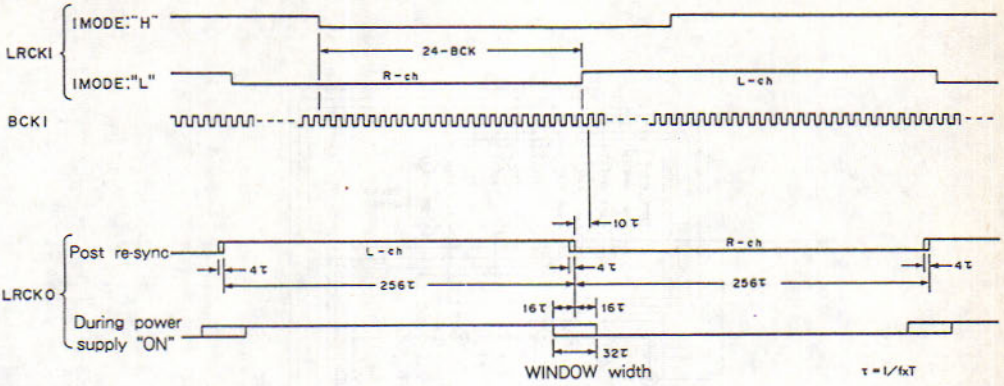
DATA Input Timing (64BCK)



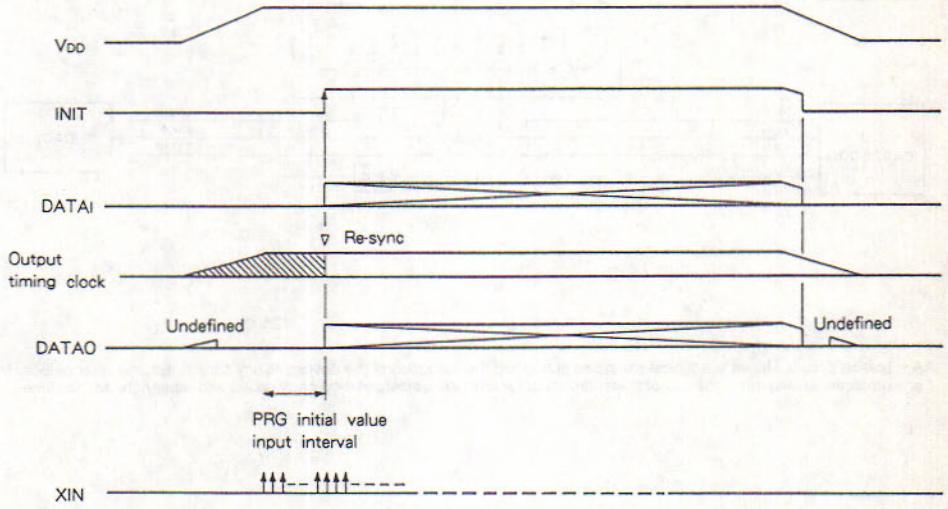
DATA Output Timing



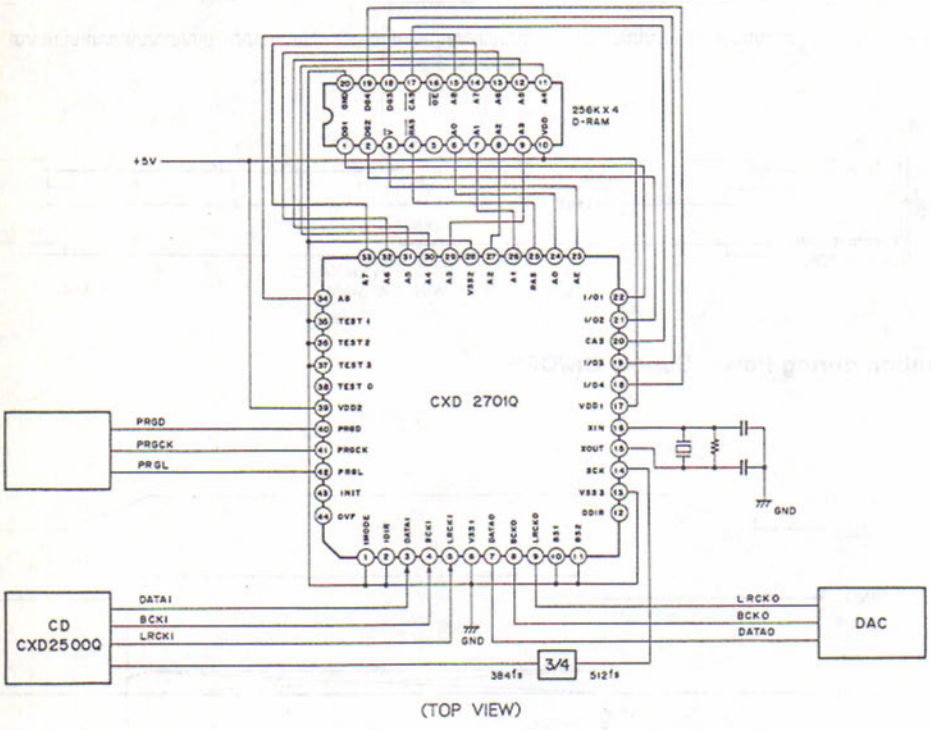
Input/Output Phases



Operation during Power Supply ON/OFF



Application Circuit

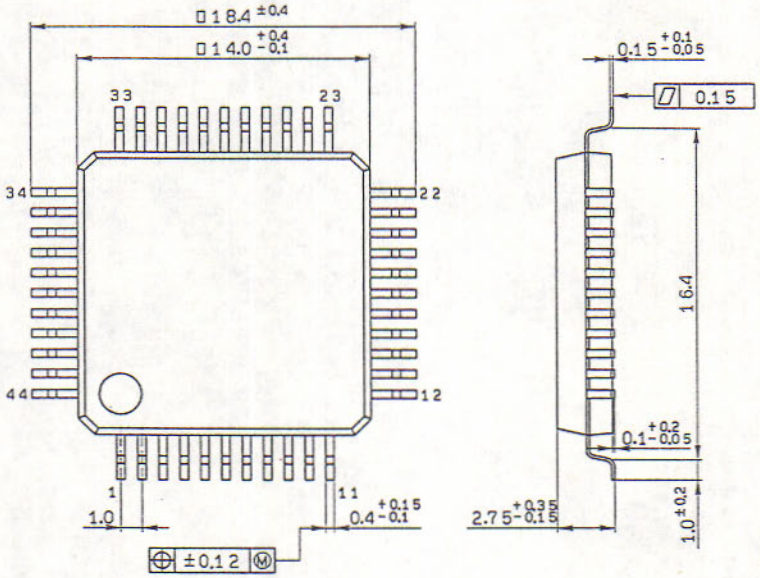


(TOP VIEW)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L01
EIAJ NAME	*QFP044-P-1414-A
JEDEC CODE	———

Digital Audio Interface IC

4) Digital Audio Interface IC

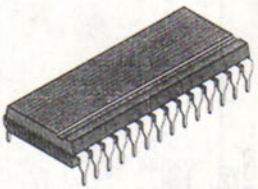
Type	Functions	Page
CXD1211P	Digital audio data modulation, Transmission	205

SONY®

CXD1211P

Digital Audio Data Modulation and Transmission IC

28 pin DIP (Plastic)



Description

CXD 1211P is an LSI to be used in consumer use for transmitting digital audio data.

Features

- Channel Status Data can be set in parallel at the input terminals, permitting the LSI to be easily connected to various digital audio system.
- Four different frequencies, 128Fs, 192Fs, 256Fs and 384Fs, can be selected for the master clock.
- Dual inputs are provided for each of Digital Audio Data and Channel Status Data C2 bit.

Structure

Silicon gate CMOS IC

Application Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}*	$V_{SS}-0.5$	to	$+7.0$	V
• Input voltage	V_I*	$V_{SS}-0.5$	to	$V_{DD}+0.5$	V
• Output voltage	V_O*	$V_{SS}-0.5$	to	$V_{DD}+0.5$	V
• Operating temperature	T_{opr}	-20	to	$+75$	°C
• Storage temperature	T_{stg}	-55	to	$+150$	°C

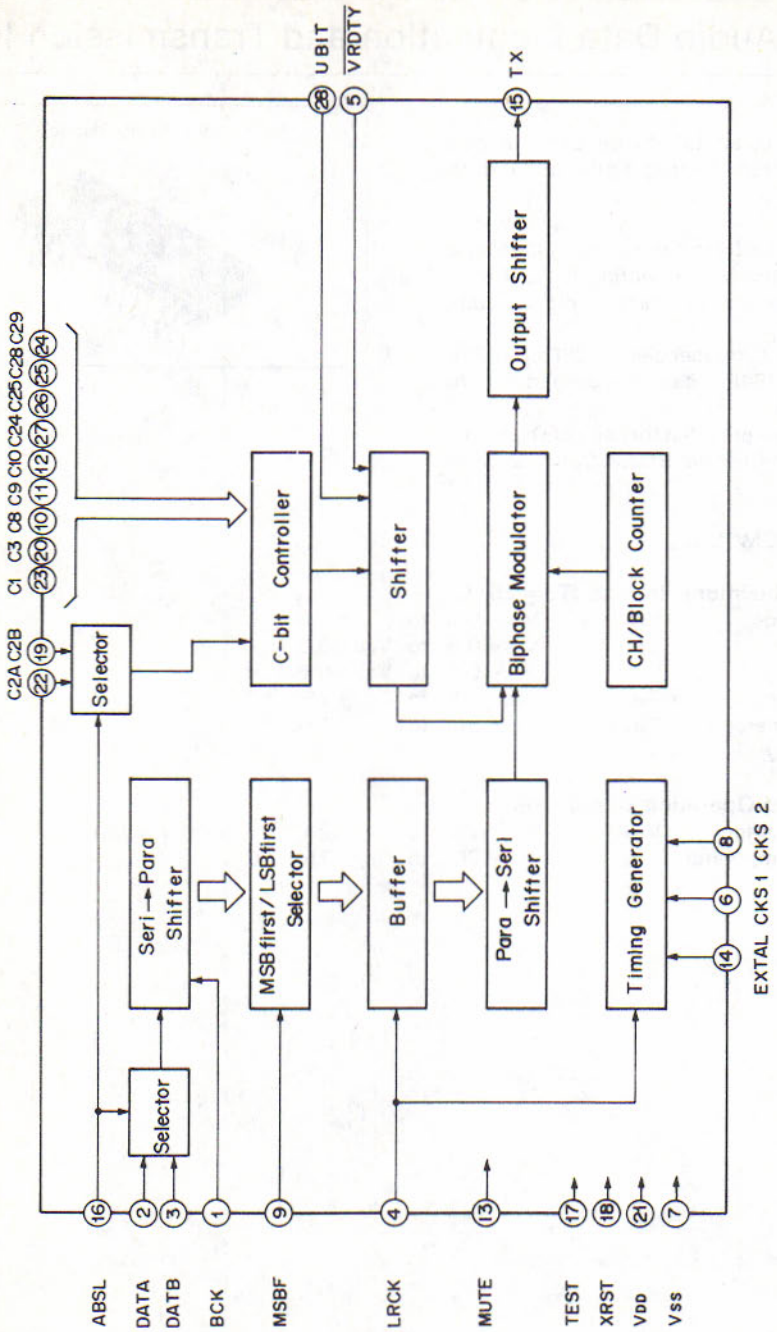
***Note)** Vss = 0V

Recommended Operating Conditions

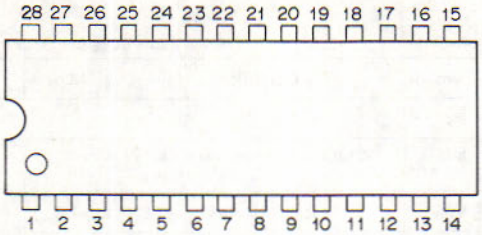
• Operating voltage	V_{DD}	4.75	to	5.25	V (5.00 V Typ.)
• Operating temperature	T_{opr}	-20	to	$+75$	°C

E91793-YA

Block Diagram



Pin Configuration (Top View) and Description



No.	Symbol	I/O	Description
1	BCK	I	Bit clock input. Data is taken in at rising edge.
2	DATA	I	Digital audio data input 1 (NRZ).
3	DATB	I	Digital audio data input 2 (NRZ).
4	LRCK	I	LR clock input. "H": L channel "L": R channel
5	$\overline{\text{VRDTY}}$	I	Validity flag input. "H" is input when data is processed for interpolation, etc.
6	CKS1	I	Frequency selection input 1 for clock to EXTAL. 192Fs, 384Fs/$\overline{\text{128Fs}}$, 256Fs
7	Vss	—	GND
8	CKS2	I	Frequency selection input 2 for clock to EXTAL. 256Fs, 384Fs/$\overline{\text{128Fs}}$, 192Fs
9	MSBF	I	MSB first/$\overline{\text{LSB first}}$ selection input for DATA and DATB.
10	C8	I	Preset input of channel status data bit 8.
11	C9	I	Preset input of channel status data bit 9.
12	C10	I	Preset input of channel status data bit 10.
13	MUTE	I	Muting input. "H": Only the audio data on TX will be 0.
14	EXTAL	I	Clock input. The frequency is selected from 128Fs/192Fs/256Fs/384Fs at CKS1 (pin 6) and CKS2 (pin 8).
15	TX	O	Output of transmitting data converted in digital audio interface format.
16	ABSL	I	Selection input of DATA (pin 2)/$\overline{\text{DATB (pin 3)}}$ and C2 (pin 22)/$\overline{\text{C2B (pin 19)}}$
17	TEST	I	Test mode set input. Fixed to "L" in normal use.
18	XRST	I	Reset input. Fixed to "H" during operation.
19	C2B	I	Preset input 2 of Channel Status Data bit 2.
20	C3	I	Preset input of Channel Status Data bit 3.
21	V_{DD}	—	+5V
22	C2A	I	Preset input 1 of Channel Status Data bit 2.
23	C1	I	Preset input of Channel Status Data bit 1.
24	C29	I	Preset input of Channel Status Data bit 29.
25	C28	I	Preset input of Channel Status Data bit 28.
26	C25	I	Preset input of Channel Status Data bit 25.
27	C24	I	Preset input of Channel Status Data bit 24.
28	UBIT	I	User Data input.

Electrical Characteristics

DC characteristics

V_{DD} = 5V ± 5%, V_{SS} = 0V, Topr = −20 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			15		mA
		I_{DSS}	Static condition $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$			0.1	
Output voltage	High level	V_{OH}	I_{OH} = −0.4mA	4.0		V_{DD}	V
	Low level	V_{OL}	I_{OL} = 2.0mA	V_{SS}		0.4	V
Input voltage	High level	V_{IH}		2.4			V
	Low level	V_{IL}				0.8	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	−10		10	μA

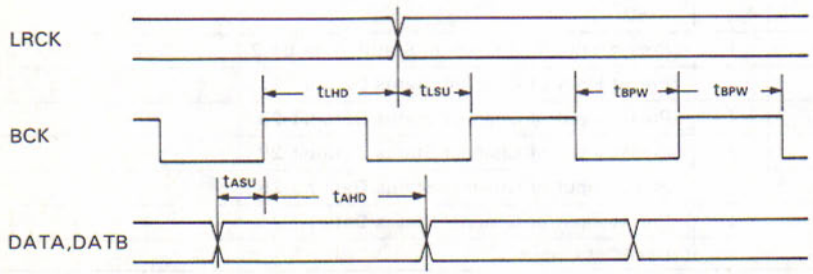
I/O capacitances

Ta = 25°C, V_{DD} = V_I = 0V, fM = 1MHz

Item	Symbol	Min.	Typ.	Max.	Unit
Inputs	C_{IN}			9	pF
Outputs	C_{OUT}			9	pF

AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
LRCK to BCK set-up time	t_{LSU}	50			ns
LRCK to BCK hold time	t_{LHD}	50			ns
DATA/DATB to BCK set-up time	t_{ASU}	50			ns
DATA/DATB to BCK hold time	t_{AHD}	50			ns
BCK pulse width	t_{BPW}	100			ns
EXTAL frequency	f_{EXT}			18.5	MHz



Description of Functions

Digital audio data input

Two input formats, MSB first mode and LSB first mode, provided for digital audio data and can be selected at the MSBF input (pin 9). (See Fig. 2.)

1) MSB first mode (MSBF = "H")
   BCK: 16 clocks/word or more
   DATA, DATB: MSB first, 16 bits from the last
2) LSB first mode (MSBF = "L")
   BCK: 24 clocks/word or more
   DATA, DATB: LSB first, 16 bits from the last

Validity flag and user data

As the validity Flag and User Data are taken in at the last BCK of each word of Digital Audio Data, input the value correponding to each word at $\overline{\text{VRDTY}}$ (pin 5) or UBIT (pin 28) as shown in Fig. 2.

The recieved user data can be transmitted as it is by connecting the UBIT input of this IC to the UBIT output of a receive/demodulation IC, CX23053 or CXD1076P.

Channel status data

In Channel Status Data, bit 0, 6 and 7 are fixed to 0, corresponding to Mode 0 of consumer use. In bit 0 to 191, this IC permits the following 10 bits to be set; Bit 1, 2, 3, 8, 9, 10, 24, 25, 28 and 29. Set these bits in parallel at the respective inputs.

With these bits, the following items can be determined.

a. Digital data/Audio data
b. Emphasis On/Off
c. Digital copy enable/disable
d. Category codes (up to 8 kinds)
e. Sampling frequency 44.1 kHz/48 kHz/32 kHz
f. Clock accuracy level I/II/III

Dual input selection

This IC is equipped with pairs of inputs for Digital Audio Data (DATA/DATB) and Channel Status Data bit 2 (C2A/C2B). These inputs can be switched at the ABSL input (pin 16). As the input at ABSL is sampled with LRCK in the IC, Digital Audio Data is not switched within the same single sample.

This function is especially effective when inputting TV main audio and additional sub audio to the two different inputs of satellite broadcast tuners.

Muting function

By setting the input at MUTE (pin 13) to "H," the audio data on the TX output (pin 15) can be set to 0 while keeping the Channel Status Data and User Data unchanged. As the input at MUTE is also sampled with LRCK inside the IC, the data is muted with 1 LRCK as a unit.

EXTAL (pin 14) frequency

The clock to be input to EXTAL can be selected from four frequencies at CKS2 (pin 6), CKS2 (pin8) as shown below.

Table 1 Clock frequency

CKS1	CKS2	EXTAL frequency
0	0	128Fs
1	0	192Fs
0	1	256Fs
1	1	384Fs

When inputting 192Fs to EXTAL, note that the output at TX may have jitters depending on the clock duty. (See Fig. 1)

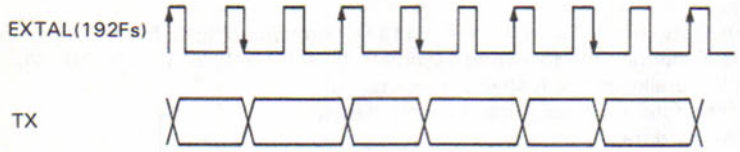


Fig. 1. TX when inputting 192Fs clock to EXTAL

Input Timing Charts

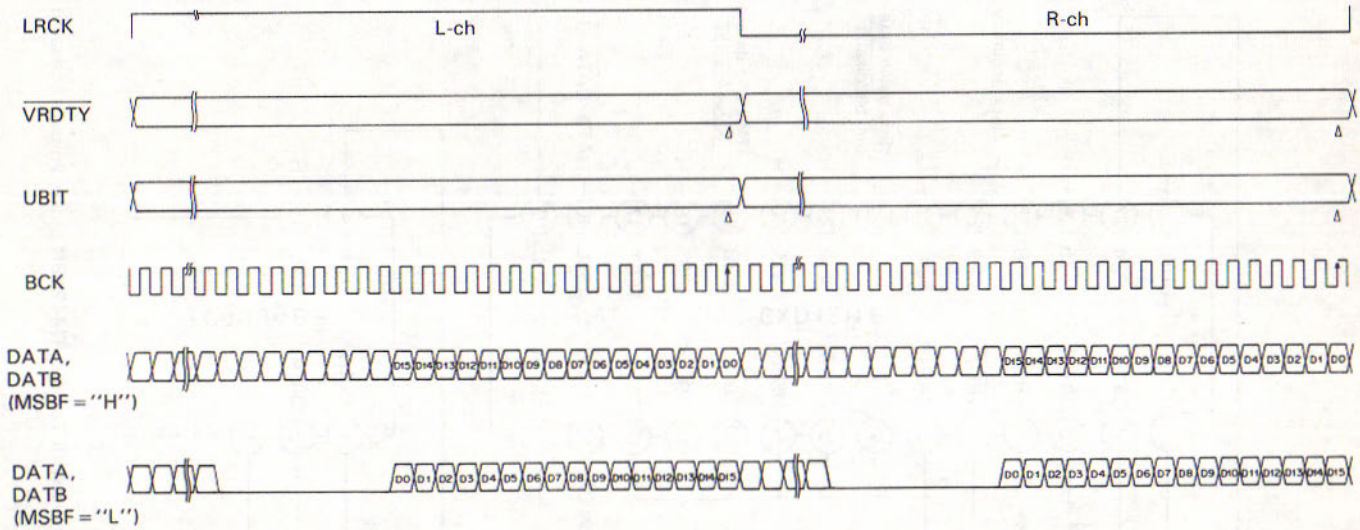
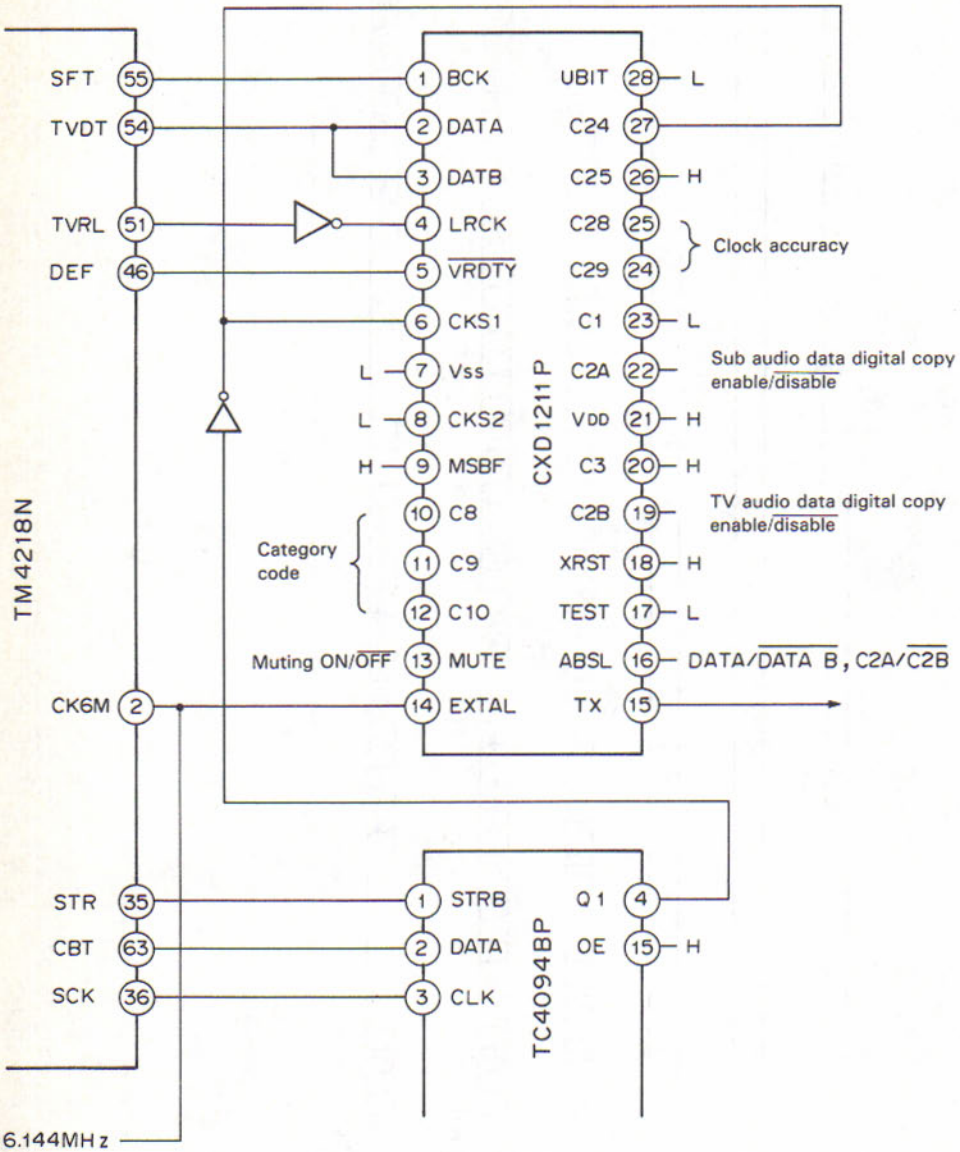


Fig. 2

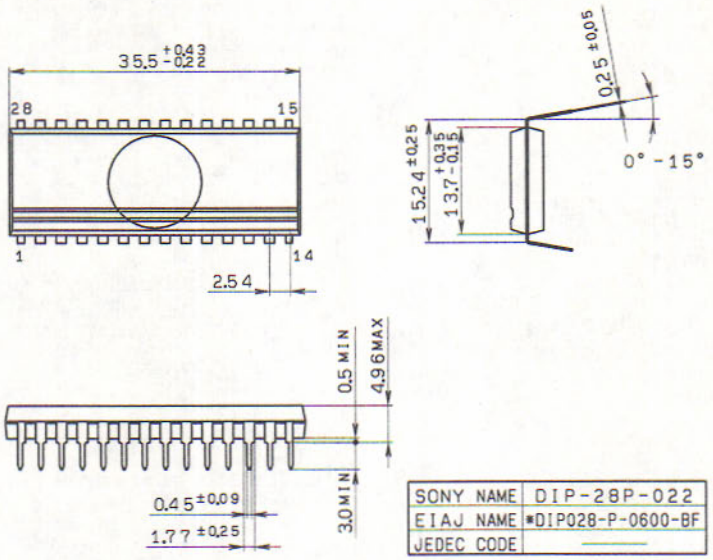
Application Circuit



Connection example with Toshiba TM4218N audio signal processing IC for B.S. Tuner.

Package Outline Unit: mm

28pin DIP (Plastic) 600mil 4.0g



SONY NAME	DIP-28P-022
EIAJ NAME	*DIP028-P-0600-BF
JEDEC CODE	

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